Analysis of Abnormal GIDL Current Degradation Under Hot Carrier Stress in DSOI-MOSFETs

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***Abstract*— It is generally believed that the gate-induced drain leakage (GIDL) current would increase with the hot carrier stress (HCS) time. As more interface electron traps are generated near the drain side, it results in a steeper energy barrier that makes the band-to-band tunneling (BTBT) process much easier. In this work, however, an abnormal decrease of such leakage current was observed in double silicon on insulator MOSFET under floating body (FB) condition. Through systematic characterization on different devices and operation conditions, we find that this behavior can be explained by the activation of lateral parasitic bipolar transistor (PBT), and the subsequent reduction of its current gain after the stress cycle. This is further supported by the simulation results that the induced additional traps would lower the amplified current by increasing the electron recombination rate. Our findings would shed more light on the roles of interface traps played in the MOSFET reliability analysis.**

***Index Terms*— Gate-induced drain leakage (GIDL) current, hot carrier stress (HCS), parasitic bipolar transistor (PBT).**

I. Introduction

With the continuous scaling of MOSFET, the OFF-state leakage current increases significantly, resulting in the ever-increasing static power consumption [1]. Many novel device structures have been proposed in advanced technology nodes to suppress this trend, including multigate structure [2], silicon-on-insulator (SOI) substrate [3], junctionless device [4], etc. Recently, double SOI (DSOI) substrate has attracted much attentions due to its improved isolation capability as compared to the conventional single SOI counterpart [5]. As illustrated in Fig. 1(a), DSOI, with another buried oxide, can effectively isolate the MOSFET on top from the bulk substrate, eliminating any crosstalk from other circuitry components. This added flexibility is very promising in realizing 3-D fin waveguide fabrication [6], high resolution detectors [7], [8] and even *in situ* sensing applications [9].

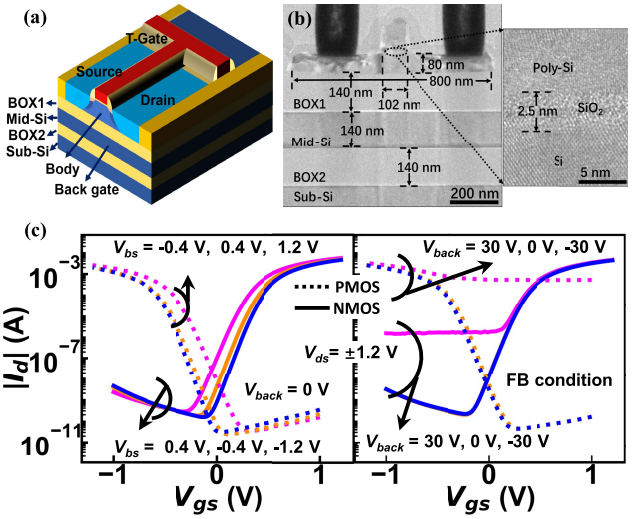

Fig. 1. (a) Schematic of DSOI-MOSFET with five terminals, including source, drain, T-gate, body, and back gate. (b) Cross-sectional TEM image of nMOS for device dimension illustration. (c) Typical I_d versus V_{gs} curves of nMOS (solid line) and pMOS (dashed line) with different V_{bs} and V_{back} biases.

Gate induced drain leakage (GIDL) current (I_{GIDL}) is a dominant OFF-state leakage component that has been intensively studied in bulk Si MOSFET [10], SOI-MOSFET [11], FinFET [12], etc. It mainly arises from the band-to-band tunneling (BTBT) in the gate–drain overlapped region, and therefore intuitively relies on the interface traps induced by hot carrier stress (HCS) [13]. Normally, I_{GIDL} would increase upon stressing since these additional traps would give rise to a steeper energy barrier that facilitates the BTBT process [14], [15], [16].

Yet, some recent works reported a contradictory descending dependence of I_{GIDL} on stress time. In particular, Ceccarelli *et al.* [17], [18] observed this abnormal trend in the bulk oxide of high-κ metal gate MOSFET underdrain avalanche hot carrier (DAHC) stress condition. It is attributed to the hole trapping caused by either vacancy-interstitial oxide

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TABLE I
COMPARISON OF THE FRESH DEVICE PERFORMANCE PARAMETERS

Device	DSOI				SOI			
Type	NMOS		PMOS		NMOS		PMOS	
Body terminal	FB	BG	FB	BG	FB	BG	FB	BG
V_{th} (V)	0.40	0.39	-0.36	-0.44	0.37	0.37	-0.41	-0.46
I_{on}/I_{off}	5.1×10^4	5.7×10^5	1.9×10^5	2.6×10^6	1.36×10^4	1.24×10^5	3.8×10^5	4.2×10^6
SS (mV/dec)	91	92	74	97	95	97	77	98
G_{mmax} (mS)	2.4	2.4	0.7	0.95	2.5	2.5	1.0	0.93

TABLE II
APPLIED VOLTAGE BIASES IN THE MSM SEQUENCE

Symbol	Definition	NMOS ($V_{dd} = 1.2$ V)	PMOS ($V_{dd} = -1.2$ V)
$V_{dstress}$	Drain voltage during stress cycle	2.4 V	-2.4 V
$V_{gstress}$	Gate voltage during stress cycle	2.4 V	-2.4 V
$V_{gs,start}$	Starting gate voltage during measurement cycle	-1 V	1 V
$V_{gs,end}$	Stopping gate voltage during measurement cycle	1.2 V	-1.2 V
V_{bs}	Body terminal connecting condition	BG (0 V), FB	BG (0 V), FB
V_{back}	Back gate voltage applied all the time	0 V	0 V
V_s	Source voltage applied all the time	Grounded (0 V)	Grounded (0 V)

defects [19] or by the diffusion of the metal gate ions in the HfO_2 itself [20]. This explanation is further supported by Dai *et al.* [21] and Tsai *et al.* [22] that a thinner HfO_2 can result in a less descending trend of I_{GIDL} due to the decrease of trapping sites. However, it remains to be clarified whether the hole trapping scenario occurs universally in MOSFET devices with different gate stacks (e.g., Polysilicon/SiO_2) or under other stress conditions (e.g., channel hot carrier (CHC) stress when the hole injection is suppressed) [23], [24], [25].

In this work, we extend the study to the DSOI MOSFETs under floating body (FB) and body grounded (BG) operation conditions that are widely employed in integrated circuits. The results show an unexpected decreasing I_{GIDL} with HCS time in nMOS under FB condition, while it keeps increasing in nMOS under BG condition and pMOS. With the assistance from technology computer-aided design (TCAD) simulation, this abnormal trend is found to correlate with the parasitic bipolar transistor (PBT) effect that is only evident in FB condition. Consequently, I_{GIDL}, in this case, is dominated by the electron emission current from PBT, which is further lowered by an enhanced electron recombination with the presence of additional HCS-induced interface traps. Our findings show that it is of significant importance to take MOSFET operation conditions into account in the analysis of GIDL current degradation.

II. EXPERIMENT SETUP

All characterized DSOI-MOSFETs were fabricated by the processes described in previous work [26]. Fig. 1(b) shows an example of cross-sectional transmission electron microscope (TEM) image of nMOS to illustrate the device dimension. The device channel length is 102 nm and the gate-stack is Polysilicon/SiO_2. The thickness of gate oxide, top silicon, middle silicon, and two buried oxide (BOX1 and BOX2) is 2.5, 80, 140, and 140 nm, respectively. The device operation voltage (V_{dd}) of nMOS (pMOS) is 1.2 (-1.2) V. As shown in Fig. 1(c), the typical $|I_d|$ versus V_{gs} curves of DSOI-MOSFET can be controlled by both body (V_{bs}) and back biases (V_{back}). As further tabulated in Table I, the fresh device performances, in terms of threshold voltage (V_{th}), ON-OFF ratio (I_{ON}/I_{OFF}), subthreshold swing (SS) and transconductance (G_{mmax}), are comparable to single SOI-MOSFET fabricated using similar processes.

The HCS measurements were performed using Keysight 1500 A semiconductor analyzer. As tabulated in Table II, measurement-stress-measurement (MSM) sequence was adopted for accelerated aging test with constant $V_{gstress}$ and $V_{dstress}$ during stress cycle. In particular, $V_{dstress}$ should be less than 80% of the drain to source breakdown voltage determined at 3.7 V. Also considering that $V_{gstress}$ should be larger than the device operation voltage (V_{dd}) of 1.2 V, $V_{dstress} = 2.4$ V is thus the minimum bias value preferred for an extended stress time. Accordingly, the bias condition for CHC is $V_{gstress} = V_{dstress} = 2.4$ V, and that for DAHC is $V_{gstress} = 0.5V_{dstress} = 1.2$ V. To exclude any hole trapping process that may complicate the discussion, hereafter we mainly focus the analysis on the results obtained under CHC condition unless otherwise specified. Between two stress cycles, the measurement cycle takes place when V_{gs} was swept from $V_{gs,start}$ to $V_{gs,end}$ with fixed $V_{ds} = V_{dd}$. In particular, V_{bs} is either grounded (0 V) or floating for

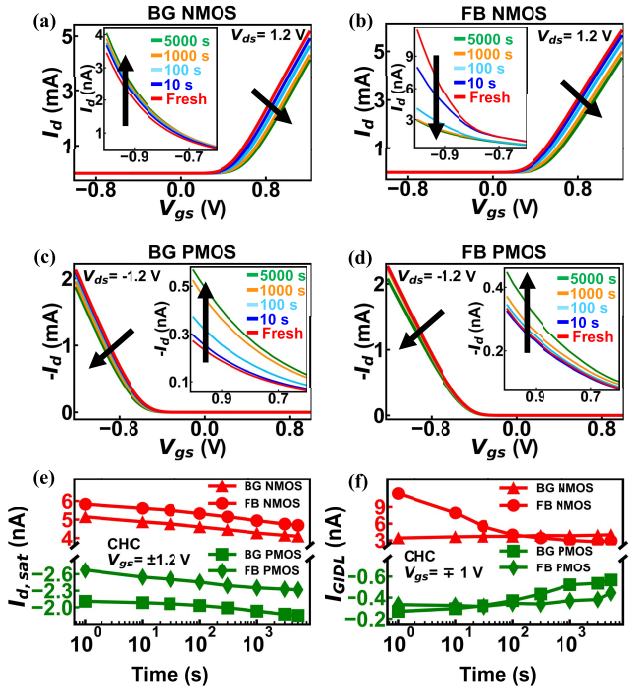

Fig. 2. (a) and (b) I_d versus V_{gs} curves of nMOS at different CHC stress time under BG and FB condition, respectively. (c) and (d) $-I_d$ versus V_{gs} curves of pMOS at different CHC stress time under BG and FB condition, respectively. (e) and (f) Stress time dependence of $I_{d,sat}$ and I_{GIDL}, respectively. Insets in (a)–(d) are the zoomed-in curves at OFF-state region.

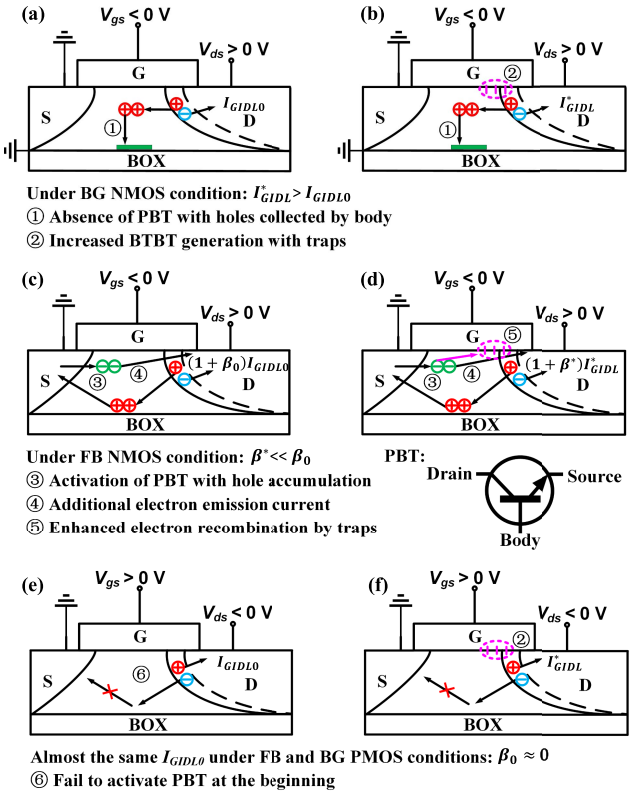

Fig. 3. Schematics of nMOS under BG condition (a) before and (b) after stress. For comparison, schematics of the PBT effect in nMOS under FB condition (c) before and (d) after stress. Schematics of pMOS under FB and BG conditions with suppressed PBT (e) before and (f) after stress.

BG or FB case while V_{back} and V_s are always kept at 0 V throughout the sequence. The total stress time is 5000 s. Drain current (I_d) with $V_{ds} = V_{dd}$ in the OFF-state region is treated as I_{GIDL} as other leakage components (e.g., junction leakage) can be generally negligible [27].

III. Result and Discussion

Fig. 2(a)–(d) show the CHC stress evolution of I_d ($-I_d$) versus V_{gs} for nMOS (pMOS) under BG and FB conditions, respectively. The OFF-state regions are enlarged in the insets for clarity. More quantitatively, the degradation dependence of ON-state saturation current ($I_{d,sat}$) and OFF-state I_{GIDL} are extracted and plotted in Fig. 2(e) and (f). As can be seen, $I_{d,sat}$ always decreases with stress in all cases due to the mobility and threshold voltage degradation, in accordance with other reports [28], [29], [30]. The degradation is even more severe in nMOS than pMOS, which can be understood as the increased difficulty in hole injection due to its higher energy thresholds than electron injection [25]. On the other hand, the dependence of I_{GIDL} relies on the specific operation condition. It monotonously increases with stress time in both nMOS and pMOS under BG condition. This agrees with the conventional view that the HCS-induced interface traps can act electrostatically on the BTBT energy barrier, leading to a steeper barrier height for an easier electron-hole pair generation [31]. It should be noted that bulk traps can also be induced by HCS, affecting the overall device degradation behavior [32], [33]. While the exact type of traps cannot be distinguished in our measurements, and their influences on I_{GIDL} are reported to be similar as the interface ones [34]. Therefore, for convenience, only the interface traps are referred to throughout this work following the convention generally accepted in [13] and [14]. As further illustrated in Fig. 3(a) and (b) for nMOS with $V_{gs} < 0$ and $V_{ds} > 0$ under BG condition, the additionally generated holes are collected by body (process 1), and the increased amount of electrons eventually gives a larger I^*_{GIDL} (aged device) than I_{GIDL0} (fresh device) (process 2).

However, under FB condition, it is surprising to find an abnormal decrease of I_{GIDL} in nMOS. And moreover, although it remains increasing in FB pMOS, the degradation is much milder than that in BG pMOS. This obvious contradiction cannot be simply explained by the hole trapping during the stress cycle and motivates us to look into the subtle differences between operation conditions. Therefore, it is still not very clear about the mechanisms of I_{GIDL} decreasing and thus motivates us to look into the subtle differences between operation conditions. Unlike the BG condition, the BTBT generated additional holes could accumulate in the body until turning on the source-body junction under FB condition [process 3 in Fig. 3(c) and (d)]. Consequently, the source would start emitting electrons into the body that are eventually collected by the drain (process 4). This gives an amplification of I_{GIDL} by a factor of $1+\beta$ (i.e., the PBT effect), where β is the PBT current gain. With the introduction of interface traps by stress, the electron recombination would increase, which makes the amplification β^* (aged device) much less than β_0 (fresh device) (process 5). Since β_0 is usually larger than unity in short-channel device, the final I_{GIDL} in our device is thus mainly

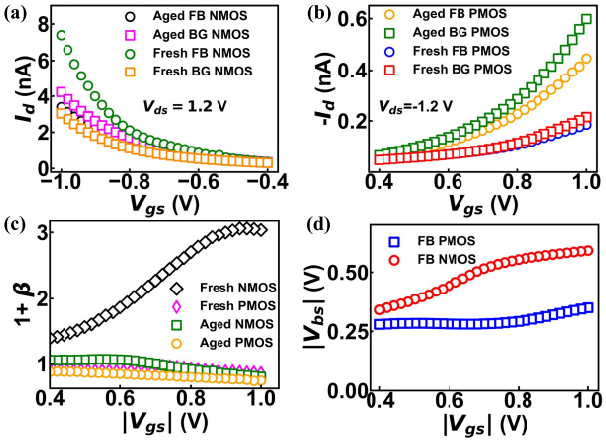

Fig. 4. (a) I_d versus V_{gs} of fresh and aged nMOS under BG and FB condition during measurement cycle using the same set of devices. (b) $-I_d$ versus V_{gs} of fresh and aged pMOS under BG and FB condition during measurement cycle using the same set of devices. (c) Estimated $1+\beta$ versus $|V_{gs}|$ of nMOS and pMOS before and after stress. (d) $|V_{bs}|$ versus $|V_{gs}|$ of nMOS and pMOS under FB condition.

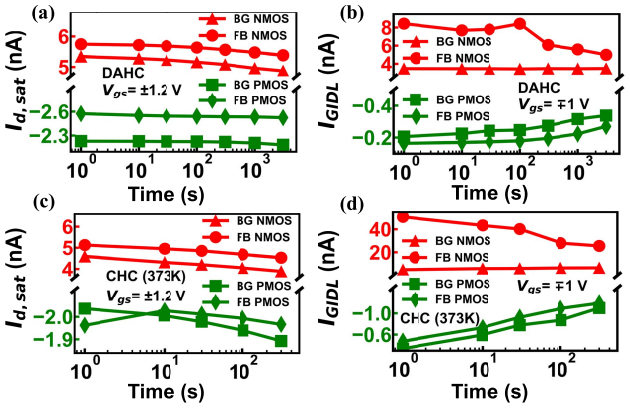

Fig. 5. Room temperature stress time dependence of (a) $I_{d,sat}$ and (b) I_{GIDL} under DAHC condition. The stress time dependence of (c) $I_{d,sat}$ and (d) I_{GIDL} under CHC condition at 373 K.

determined by the magnitude of β, and follows the decreasing trend on stress time. It should be noted that PBT effect should in principle occur in pMOS as well, but the amount of electrons accumulated in the body are too few to activate PBT [process 6 in Fig. 3(e)]. No obvious I_{GIDL} difference can be observed by comparing the results of fresh FB and BG pMOS in Fig. 2(c) and (d). In other words, β_0 is almost zero and β^* remains close to zero after HCS. Therefore, I_{GIDL} in pMOS follows the normal increasing dependence on stress time due to an increased BTBT generation [again process 2 in Fig. 3(f)]. To further confirm that the difference indeed comes from the operation conditions during measurement cycle, we measured I_d versus V_{gs} curves of nMOS [see Fig. 4(a)] and pMOS [see Fig. 4(b)] using the same set of fresh and aged devices under BG and FB conditions again. As can be seen, I_{GIDL} in the aged nMOS device is always smaller than the fresh one as long as its body is floating, while the situation becomes reversed when the body is subsequently connected to ground during the measurement. This observation undoubtedly excludes the different carrier trapping process during the stress cycle (e.g., hole trapping) as the main cause for the abnormal I_{GIDL} trend in our devices. As for pMOS, I_{GIDL} follows the same trend as in Fig. 2(c) and (d) with little discernible difference in an expected way.

For a more quantitative understanding, we argue that the PBT gain $1+\beta$ can be estimated as the ratio of I_{GIDL} obtained under FB condition to that under BG condition [see Fig. 4(c)]. This is valid since PBT is supposed to be suppressed when the body is grounded [35]. We do note that $1+\beta$ is usually extracted by the comparison of drain leakage between short- and long-channel devices [36]. While such approach is not feasible here for the HCS measurements as any hot carrier-related process is highly bound to the device dimensions [37]. It is not possible for aged devices of different channel lengths to have similar trap distributions and thus preventing an accurate $1+\beta$ extraction. Although our as-obtained $1+\beta$ can also be underestimated due to the lowered lateral electric field under FB condition [38], we can find that it is still quite large in fresh nMOS with the presence of PBT, and gets reduced to a small value around unity after stress. In contrast, it is always around unity before and after stress in pMOS where no sizable PBT is present. By experimentally monitoring the body potential ($|V_{bs}|$) during $|V_{gs}|$ sweeping in Fig. 4(d), we confirm the appearance of strong hole accumulation in the nMOS body with the increase of $|V_{bs}|$; whereas the almost constant $|V_{bs}|$ in pMOS implies the rather weak electron accumulation. These additional measurement results in Fig. 4 demonstrate that the abnormal I_{GIDL} dependence is indeed originated from the PBT effect and the stress-induced current gain reduction.

To provide more evidences, we also checked the degradation behavior under DAHC condition or at an elevated temperature. As summarized in Fig. 5(a), $I_{d,sat}$ under DAHC condition keeps decreasing as the stress time evolves in all cases. Again, the abnormal decreasing I_{GIDL} in Fig. 5(b) is only observed in FB nMOS, while the rest exhibit the normal increasing dependence. Moreover, the extracted results in Fig. 5(c) and (d) also show that there is generally no qualitative difference for the $I_{d,sat}$ and I_{GIDL} dependence under CHC at 373 K as compared to the room temperature ones. Any difference with Fig. 2(e) and (f) is more of a quantitative nature. In particular, both I_{GIDL} and the associated initial PBT current gain β_0 increase with the rise of temperature, in agreement with other previous studies [39]. Nonetheless, β_0 still decreases upon the application of HCS, eventually leading to the decrease of I_{GIDL} as illustrated in Fig. 3(c) and (d). These additional experimental results in Fig. 5 demonstrate again that the abnormal I_{GIDL} trend is closely related to the PBT current gain. As long as a sizable β_0 (much larger than unity) exists in fresh devices, this type of decreasing I_{GIDL} dependence can be robustly observed. In fact, we also obtained similar results in conventional single SOI devices fabricated using similar processes (not shown here), which confirms the universality of our proposed explanation. It is noticed that Yeh *et al.* [40] has previously reported a similar I_{GIDL} reduction in single SOI devices, and attributed to the HCS-induced drop of body to drain potential. However, according to the 2-D GIDL current model [38], this potential drop instead should lead to the increase of lateral electric field that eventually increases I_{GIDL} through an enhanced BTBT process. With all the experimental results presented above, we,

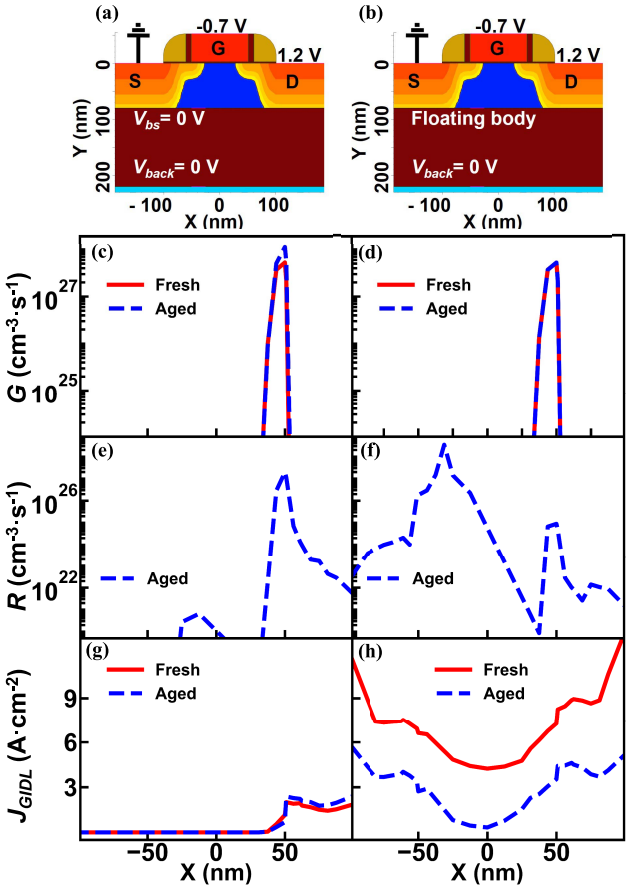

Fig. 6. (a) and (b) Doping concentration and OFF-state bias conditions of nMOS used in simulation. (c) and (d) BTBT generation rate (G). (e) and (f) eGapStatesRecombination rate (R = 0 in fresh device). (g) and (h) GIDL current density (J_{GIDL}) along the Si-SiO_2 interface for BG and FB condition before and after stress, respectively.

therefore, believe that it is more attempting to invoke the PBT effect to account for the abnormal I_{GIDL} dependence on HCS.

To further reveal the underlying factors contributing to the reduction of $1+\beta$, the influence of PBT on I_{GIDL} upon stressing was investigated using commercial TCAD simulator. The doping concentration and OFF-state bias conditions of the simulated nMOS are presented in Fig. 6(a) and (b). We set zero traps for the fresh device, and the HCS degradation model with $V_{dstress} = V_{gstress} = 2.4$ V was employed under 5000 s transient simulation to generate interface traps [41] for the aged one. The influence of these traps are considered from the following aspects in the simulation: 1) an increased BTBT generation from the increase of the electric field near the drain side [42]; 2) an enhanced recombination with electrons along the channel [43]; and 3) a degraded mobility by severer Coulomb scattering [44]. Consequently, for a qualitative comparison, Fig. 6(c)–(h) plot the obtained BTBT generation rate (G), eGapStatesRecombination rate due to traps (R) and OFF-state leakage current density (J_{GIDL}) extracted along Si-SiO_2 interface ($Y = 0$). The increase of I_{GIDL} under BG condition after stress [see Fig. 6(g)] can indeed be attributed to the slight G increase [see Fig. 6(c)]. In contrast, there is no discernible change in G when the body is floating [see Fig. 6(d)]. Instead, as shown in Fig. 6(e) and (f), R increases dramatically under FB condition after stress; while it is still quite small under BG condition due to the fewer electron flux in the lateral channel. It should be noted that since it only accounts for the recombination rate by traps [45], R is automatically equal to zero when we set zero traps in the fresh device. Therefore, it is this increased surface recombination in aged device that lowers the electron emission current and eventually leads to the decrease of $1+\beta$ and I_{GIDL} [see Fig. 6(h)].

IV. Conclusion

In summary, an abnormal decrease of I_{GIDL} dependence on HCS was observed in DSOI-MOSFETs under FB condition. Through combined experimental and TCAD analysis on different devices and operation conditions, we verify that the origin is related to the activation of PBT effect by hole accumulation in the body. Consequently, the HCS-induced interface traps would weaken the PBT effect through enhanced recombination with emission electron from the source, which eventually results in the descending I_{GIDL} trend. Our work unveils an alternative influence of the HCS-induced interface traps on GIDL degradation that has often been overlooked and elucidates its abnormal degradation trend especially in the advanced short channel devices where PBT is hard to be fully suppressed [46], [47], [48].

References

[1] V. De and S. Borkar, "Technology and design challenges for low power and high performance [microprocessors]," in *Proc. Int. Symp. Low Power Electron. Design*, 1999, pp. 163–168, doi: 10.1109/LPE.1999.799433.

[2] A. K. Dadori, K. Khare, T. K. Gupta, and R. P. Singh, "Leakage power reduction technique by using multigate FinFET in DSM technology," in *Proc. Int. Conf. Commun. Syst. Netw.*, 2017, pp. 233–244, doi: 10.1007/978-981-10-2750-5_25.

[3] J. Cai *et al.*, "Will SOI have a life for the low-power market?" in *Proc. IEEE Int. SOI Conf.*, Oct. 2008, pp. 15–16, doi: 10.1109/SOI.2008.4656272.

[4] M. K. Rai, A. Gupta, and S. Rai, "Comparative analysis & study of various leakage reduction techniques for short channel devices in junctionless transistors: A review and perspective," *Silicon*, vol. 14, no. 9, pp. 4423–4445, Jun. 2022, doi: 10.1007/s12633-021-01181-6.

[5] G. Chuang *et al.*, "DSOI—A novel structure enabling adjust circuit dynamically," *J. Semiconductors*, vol. 37, no. 6, Jun. 2016, Art. no. 065003, doi: 10.1088/1674-4926/37/6/065003.

[6] J. Byers *et al.*, "Silicon slot fin waveguide on bonded double-SOI for a low-power accumulation modulator fabricated by an anisotropic wet etching technique," *Opt. Exp.*, vol. 26, no. 25, pp. 33180–33191, 2018, doi: 10.1364/OE.26.033180.

[7] R. Bugiel *et al.*, "High spatial resolution monolithic pixel detector in SOI technology," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 988, Feb. 2021, Art. no. 164897, doi: 10.1016/j.nima.2020.164897.

[8] M. Casalino, "Theoretical investigation of near-infrared Fabry–Pérot microcavity graphene/silicon Schottky photodetectors based on double silicon on insulator substrates," *Micromachines*, vol. 11, no. 8, p. 708, Jul. 2020, doi: 10.3390/mi11080708.

[9] M. Arsalan *et al.*, "Suppressing crosstalk in the photoelectron *in-situ* sensing device (PISD) by double SOI," in *Proc. Joint Int. EUROSOI Workshop Int. Conf. Ultimate Integr. Silicon (EUROSOI-ULIS)*, Sep. 2020, pp. 1–4, doi: 10.1109/EUROSOI-ULIS49407.2020.9365553.

[10] P. T. Lai, J. P. Xu, W. M. Wong, H. B. Lo, and Y. C. Cheng, "Correlation between hot-carrier-induced interface states and GIDL current increase in n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, no. 2, pp. 521–528, Feb. 1998, doi: 10.1109/16.658689.

[11] Y.-K. Lin *et al.*, "Modeling of back-gate effects on gate-induced drain leakage and gate currents in UTB SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 3986–3990, Oct. 2017, doi: 10.1109/TED.2017.2735455.

[12] C. K. Dabhi, A. S. Roy, L. Yang, and Y. S. Chauhan, "Anomalous GIDL effect with back bias in FinFET: Physical insights and compact modeling," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3261–3267, Jul. 2021, doi: 10.1109/TED.2021.3083483.

[13] B. Zhang, A. Balasinski, and T. P. Ma, "Hot-carrier effects on gate-induced-drain-leakage (GIDL) current in thin-film SOI/NMOSFET's," *IEEE Electron Device Lett.*, vol. 15, no. 5, pp. 169–171, May 1994, doi: 10.1109/55.291597.

[14] F.-M. Ciou *et al.*, "Investigation of HCD- and NBTI-induced ultralow electric field GIDL in 14-nm technology node FinFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 7, pp. 2697–2701, Jul. 2020, doi: 10.1109/TED.2020.2992004.

[15] T.-E. Chang, C. Huang, and T. Wang, "Mechanisms of interface trap-induced drain leakage current in off-state n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 42, no. 4, pp. 738–743, Apr. 1995, doi: 10.1109/16.372079.

[16] T. Wang, L.-P. Chiang, N.-K. Zous, C.-F. Hsu, L.-Y. Huang, and T.-S. Chao, "A comprehensive study of hot carrier stress-induced drain leakage current degradation in thin-oxide n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, no. 9, pp. 1877–1882, Sep. 1999, doi: 10.1109/16.784188.

[17] E. Ceccarelli, K. Manning, S. Maxwell, and C. Heffernan, "GIDL increase due to HCI stress: Correlation study of MOSFET degradation parameters and modelling for reliability simulation," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2019, pp. 1–5, doi: 10.1109/IRPS.2019.8720590.

[18] E. Ceccarelli, K. Manning, G. Macera, D. Dempsey, and C. Heffernan, "HCD-induced GIDL increase and circuit implications," in *Proc. IEEE 25th Int. Symp. Test. Robust Syst. Design (IOLTS)*, Jul. 2019, pp. 76–79, doi: 10.1109/IOLTS.2019.8854462.

[19] C. Gu, D. S. Ang, Y. Gao, R. Gu, Z. Zhao, and C. Zhu, "A vacancy-interstitial defect pair model for positive-bias temperature stress-induced electron trapping transformation in the high-κ gate n-MOSFET," *IEEE Trans. Electron Devices*, vol. 64, no. 6, pp. 2505–2511, Jun. 2017, doi: 10.1109/TED.2017.2694440.

[20] Y.-H. Lu *et al.*, "Fast-IV measurement investigation of the role of TiN gate nitrogen concentration on bulk traps in HfO_2 layer in p-MOSFETs," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 2, pp. 475–478, Jun. 2017, doi: 10.1109/TDMR.2017.2672740.

[21] C.-H. Dai *et al.*, "Hot carrier effect on gate-induced drain leakage current in high-k/metal gate n-channel metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 99, no. 1, Jul. 2011, Art. no. 012106, doi: 10.1063/1.3608241.

[22] J.-Y. Tsai *et al.*, "Hole injection-reduced hot carrier degradation in n-channel metal-oxide-semiconductor field-effect-transistors with high-k gate dielectric," *Appl. Phys. Lett.*, vol. 102, no. 7, Feb. 2013, Art. no. 073507, doi: 10.1063/1.4791676.

[23] C. Gupta, A. Gupta, and A. Dixit, "Impact of hot carrier degradation on GIDL current in 45 nm SOI-NFETs," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, Oct. 2019, pp. 1–4, doi: 10.1109/IIRW47491.2019.8989899.

[24] A. McCabe, R. G. Manley, J. G. Couillard, C. K. Williams, and K. Hirschman, "High field induced stress suppression of GIDL effects in accumulation-mode p-channel TFTs," *ECS Trans.*, vol. 33, no. 5, pp. 95–103, Oct. 2010, doi: 10.1149/1.3481223.

[25] S. Mahapatra and U. Sharma, "A review of hot carrier degradation in n-channel MOSFETs—Part I: Physical mechanism," *IEEE Trans. Electron Devices*, vol. 67, no. 7, pp. 2660–2671, Jul. 2020, doi: 10.1109/TED.2020.2994302.

[26] Y. Gao, K. Lu, Y. Chang, Z. Xue, and X. Wei, "Investigation of negative bias effect on radiation hardening for double SOI technology," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 4, pp. 908–914, Apr. 2022, doi: 10.1109/TNS.2022.3154373.

[27] X. Yuan *et al.*, "Gate-induced-drain-leakage current in 45-nm CMOS technology," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 3, pp. 501–508, Sep. 2008, doi: 10.1109/TDMR.2008.2002350.

[28] C. H.-J. Huang, T. A. Rost, and J. W. McPherson, "Degradation of off-state leakage in PMOS transistors under hot carrier injection," in *Proc. IEEE Int. Integr. Rel. Workshop (IRWS)*, 1994, pp. 63–68, doi: 10.1109/IRWS.1994.515827.

[29] Z. Yu, Z. Zhang, Z. Sun, R. Wang, and R. Huang, "On the trap locations in bulk FinFETs after hot carrier degradation (HCD)," *IEEE Trans. Electron Devices*, vol. 67, no. 7, pp. 3005–3009, Jul. 2020, doi: 10.1109/TED.2020.2994171.

[30] Y. Pan, "A physical-based analytical model for hot-carrier induced saturation current degradation of p-MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 1, pp. 84–89, Jan. 1994, doi: 10.1109/16.259624.

[31] G. Q. Lo, A. B. Joshi, and D.-L. Kwong, "Hot-carrier-stress effects on gate-induced drain leakage current in n-channel MOSFETs," *IEEE Electron Device Lett.*, vol. 12, no. 1, pp. 5–7, Jan. 1991, doi: 10.1109/55.75679.

[32] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb. 1992, doi: 10.1109/16.121690.

[33] J. C. Liao *et al.*, "Investigation of bulk traps enhanced gate-induced leakage current in Hf-based MOSFETs," *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 509–511, May 2008, doi: 10.1109/LED.2008.920286.

[34] T.-E. Chang, C. Huang, and T. Wang, "Mechanisms of interface trap-induced drain leakage current in off-state n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 42, no. 4, pp. 738–743, Apr. 1995, doi: 10.1109/16.372079.

[35] J. Chen *et al.*, "A tunnel diode body contact structure to suppress the floating-body effect in partially depleted SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1346–1348, Oct. 2011, doi: 10.1109/LED.2011.2162813.

[36] J. Chen, F. Assaderaghi, P.-K. Ko, and C. Hu, "The enhancement of gate-induced-drain-leakage (GIDL) current in short-channel SOI MOSFET and its application in measuring lateral bipolar current gain beta," *IEEE Electron Device Lett.*, vol. 13, no. 11, pp. 572–574, Nov. 1992, doi: 10.1109/55.192844.

[37] T. Grasser, *Hot Carrier Degradation Semiconductor Devices*. New York, NY, USA: Springer, 2015, pp. 111–114, doi: 10.1007/978-3-319-08994-2.

[38] S. A. Parke, J. E. Moon, H.-J. C. Wann, P. K. Ko, and C. Hu, "Design for suppression of gate-induced drain leakage in LDD MOSFETs using a quasi-two-dimensional analytical model," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1694–1703, Jul. 1992, doi: 10.1109/16.141236.

[39] G. Q. Wang *et al.*, "Revisited parasitic bipolar effect in FDSOI MOSFETs: Mechanism, gain extraction and circuit applications," *Solid-State Electron.*, vol. 185, Nov. 2021, Art. no. 108069, doi: 10.1016/j.sse.2021.108069.

[40] W.-K. Yeh, W.-H. Wang, Y.-K. Fang, and F.-L. Yang, "Temperature dependence of hot-carrier-induced degradation in 0.1 μm SOI nMOSFETs with thin oxide," *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 425–427, Jul. 2002, doi: 10.1109/LED.2002.1015228.

[41] S. Reggiani *et al.*, "TCAD simulation of hot-carrier and thermal degradation in STI-LDMOS transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 691–698, Feb. 2013, doi: 10.1109/TED.2012.2227321.

[42] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, "Subbreakdown drain leakage current in MOSFET," *IEEE Electron Device Lett.*, vol. EDL-8, no. 11, pp. 515–517, Nov. 1987, doi: 10.1109/EDL.1987.26713.

[43] R. F. Pierret and G. W. Neudeck, *Advanced Semiconductor Fundamentals*, vol. 6. Reading, MA, USA: Addison-Wesley, 1987.

[44] W. Zhu, J.-P. Han, and T. P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-k dielectrics," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 98–105, Jan. 2004, doi: 10.1109/TED.2003.821384.

[45] *Sentaurus Device User Guide Version O-2018.06, June 2018*, Synopsys, Mountain View, CA, USA, 2018.

[46] X. Zhao, A. Vardi, and J. A. del Alamo, "Excess OFF-state current in InGaAs FinFETs: Physics of the parasitic bipolar effect," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2113–2118, May 2019, doi: 10.1109/TED.2019.2903912.

[47] F. Liu, I. Ionica, M. Bawedin, and S. Cristoloveanu, "Extraction of the parasitic bipolar gain using the back-gate in ultrathin FD SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 96–98, Feb. 2015, doi: 10.1109/LED.2014.2385797.

[48] S. Sahay and M. J. Kumar, "Controlling L-BTBT and volume depletion in nanowire JLFETs using core–shell architecture," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3790–3794, Sep. 2016, doi: 10.1109/TED.2016.2591588.