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Demonstration and modeling of frequency tripler based on GaN Schottky diode pair

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ABSTRACT

Based on GaN Schottky barrier diode (SBD), frequency triplers using anti-parallel diode pair (APDP) are demonstrated and modeled at an output frequency of 3.6 GHz. In addition, two connection schemes, namely series APDP tripler and shunt APDP tripler are explicitly studied and compared. Compared to shunt APDP tripler, series APDP tripler achieved higher output power of −0.14 dBm and smaller minimum conversion loss of 26.9 dB. Precise compact models for both types of triplers were proposed to verify the generation of output power and performance of triplers. In the compact models, nonlinear SPICE parameters of SBD and parasitic parameters of the diode pair were extracted from I–V characteristic and broad band small signal S-parameters. Input and output networks of tripler were de-embedded so that accuracy of harmonic simulations were ensured. The outstanding performance of APDP as a frequency tripler and corresponding models provide a practical option in designing RF multipliers.

1. Introduction

Devices for frequency conversion, including frequency multipliers, frequency dividers, and mixers, have long been regarded as critical components in many radio frequency (RF) applications [1,2], such as radio astronomy, wireless communication, and high-quality imaging. In the broadband sliding intermediate frequency (sliding-IF) transceiver architectures, voltage controlled oscillator (VCO) is typically used to supply sufficiently large local oscillator (LO) signal for the generations of first and second IF [3,4]. However, a VCO with wide frequency tuning range and low phase noise is particularly challenging to be implemented. Thus, a frequency doubler or tripler is typically employed at the output of VCO to provide a wide tuning range and solve the pulling problem of VCO [5,6]. Recently, several reports have investigated frequency multiplication topologies to enhance the targeting harmonic while suppressing other harmonics [4,7–10]. Among them, anti-parallel diode pair (APDP) circuits have emerged as a promising candidate as frequency triplers, owing to their outstanding even-harmonics suppression capability making use of symmetric of I–V characteristic nonlinearity [11–14]. A shunt connected APDP tripler based on diodes of n- and p-type has been demonstrated to avoid the deleterious effects of parasitic capacitance to substrate and work with a high input frequency [12]. Limited working range with high efficiency of APDP triplers was found due to the fixed I–V nonlinearity. To work with different input power, a scheme of applying static bias on the n-type Schottky barrier diode (SBD) of APDP has been developed [13].

Despite the fact that APDP triplers based on SBDs using CMOS technology have been investigated amply in previous reports, there are still several concerns to be addressed, before reaching a comprehensive understanding:

1) Typically, APDP tripler could be implemented in two ways, either shunt connected APDP [12–14] or series connected APDP [15–17] in the tripler networks. Nevertheless, a performance comparison between two types of triplers is absent. An understanding of the two APDP configurations is actually paramount to achieving a good frequency tripler design.
2) Due to the relatively low barrier height of SBD in Si CMOS technology, the output power of APDP triplers typically tend to get saturated at a small input power, which leads to a limited maximum output power and the degradation of conversion efficiency as increasing the input power [12,13].

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GaN materials hold the properties of wide band gap, large electron mobility in 2-dimension electron gas (2-DEG), and high thermal conductivity [18,19]. In addition, using proper metals, relatively large Schottky barrier of AlGaN/GaN based SBDs can be achieved, which enables the outstanding capability in accommodating large input power for SBDs. Therefore, APDP triplers based on AlGaN/GaN SBDs are expected to achieve large output power.

In this work, both series connected and shunt connected APDP triplers based on GaN-on-SiC SBD pair were fabricated and thoroughly investigated. A comparison between two types of APDP triplers was also conducted in terms of output power density and conversion loss. In addition, precise compact models for both types of APDPs were proposed and simulated to verify their large signal performances. Both nonlinear parameters of SBD and parasitic parameters were extracted. Simulated small signal S-parameters and large signal performances for both triplers agreed well with the measurement results. The compact models also paved the way for system level circuit design with precision and high efficiency.

2. Experiment and tripler performances

Fig. 1(a) illustrates optical microscope photograph of a fabricated APDP, which consists of two AlGaN/GaN SBDs with the same size to achieve the symmetric I–V characteristics and perform well as a frequency tripler. The AlGaN/GaN SBDs used in this work, shown in the dashed boxes, were grown and fabricated on SiC substrate and consisted of a 25 nm AlGaN barrier layer and a 200 nm GaN buffer layer, Anode and cathode of SBDs, fabricated with Schottky contact and ohmic contact respectively, are also specified in the figure. The length of anode-to-cathode (L_{AC})/width of electrodes (W) for each SBD were 5 μm and 50 μm. The device fabrication started with mesa isolation using SiO_2 as hard mask and the AlGaN/GaN-epi was etched for 190 nm using ICP-RIE. After the mesa isolation, the device was etched with 3% TMAH at 50 °C for a smooth sidewall. The Ohmic contact was formed with 20/150/50/80 nm Ti/Al/Ni/Au and annealed at 850 °C for 45s. The contact resistance R_c and sheet resistance R_s were 1.38 Ω*mm and 417 Ω/sq, measured from transmission line structures. The Schottky gate was formed by depositing 50/200 nm Ni/Au. The diode pair was connected to Ground-Signal-Ground (GSG) probe pad directly and the corresponding equivalent circuit is shown in Fig. 1(b). Fig. 1(c) reports the I–V characteristic of APDP, which was measured by B1500A semiconductor device analyzer with a DC bias from −3 V to 3 V. Forward threshold voltage (V_{th}) of SBD in APDP at 1 mA/mm current density standard [20] was determined to be 1.06 V, and the non-conducting region (off-zone) of APDP, where none of SBDs is conducting, is illustrated in cyan region in Fig. 1(c).

The operation principles for APDP tripler are briefly summarized as follows. Assume the input sinusoidal signal of APDP is:

$$V_{RF}(t) = A_{RF}\cos(\omega_{RF}t) \tag{1}$$

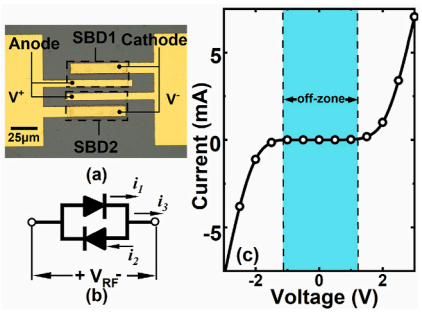

Fig. 1. (a). Optical microscope photograph, (b). Equivalent circuit, and (c). I–V characteristics of GaN based APDP topology.

where A_{RF} and ω_{RF} are the amplitude and frequency of input sinusoidal signal, respectively. Current on each SBD of APDP can be written as:

$$i_1(t) = I_s\left(\exp\left(\frac{qV_{RF}}{NkT}\right) - 1\right) \tag{2}$$

$$i_2(t) = I_s\left(\exp\left(\frac{-qV_{RF}}{NkT}\right) - 1\right) \tag{3}$$

where V_{RF} is the voltage drop on SBD, q is the electronic charge, N is ideal factor, T means the ambient temperature, I_S denotes reverse saturation current, and k the Boltzmann constant. As shown in Fig. 1(b), the total output current (i_3) of APDP can be written as the difference between $i_1(t)$ and $i_2(t)$. Taylor expansion of $i_3(t)$ for APDP then can be derived. The derivation process is illustrated in (4).

$$\begin{aligned} i_3(t) &= i_1(t) - i_2(t) \\ &= I_s\left(\exp\frac{qV_{RF}}{NkT} - \exp\frac{-qV_{RF}}{NkT}\right) \\ &= 2I_s\sinh\left(\frac{qA_{RF}}{NkT}\cos(\omega_{RF}t)\right) \\ &= 2I_s(\alpha_1\cos(\omega_{RF}t) + \alpha_3\cos(3\omega_{RF}t) \\ &= +\alpha_5\cos(5\omega_{RF}t) + \ldots) \end{aligned} \tag{4}$$

According to (4), output signal of APDP only contains the odd harmonic components, while even harmonics are intrinsically inhibited by the topology. The very property makes APDP be a promising choice in frequency tripling.

As shown in Fig. 2, APDP based frequency tripler can be implemented by two types of connections between APDP and tripler network, which are named as series APDP tripler and shunt APDP tripler in this work, respectively. In the case of series APDP tripler, two ports of APDP are connected into network as a series component. In the case of shunt APDP tripler, one of the APDP ports is connected into network, while the other port is grounded. Fig. 2 also illustrates the measurement setup for two types of APDP triplers. The fundamental input RF signal of 1.2 GHz was fed into tripler with R&S SMA100B signal generator. An impedance tuner was connected to the output of APDP to match the output impedance of APDP at output frequency of 3.6 GHz. The output power spectrum of APDP topology was measured by R&S FSV spectrum analyzer.

Fig. 3 reports the measured output power density (PD) and conversion loss (CL), defined as PD = ($P_{out|dBm}$/Width) and CL = $|P_{out|dBm} - P_{in|dBm}|$, as functions of input power for both types of APDP triplers with output frequency of 3.6 GHz. As increasing input power, output PD of both types of triplers showed a rapid increase until input power reached 20 dBm and then the slope of PD was slightly compromised. Measured maximum output PD for series APDP and shunt APDP were −16.7 dBm/μm and −23.6 dBm/μm at input power of 28 dBm, respectively. The corresponding minimum conversion loss were determined to be 26.9 dB and 34.3 dB at input power of 25 dBm. Among two triplers, series APDP tripler achieved a max output power of −0.14 dBm, which was much larger than APDP triplers based on Si CMOS technology in the literatures [12,13]. It was attributed to the relatively wider off-zone in I–V curve of

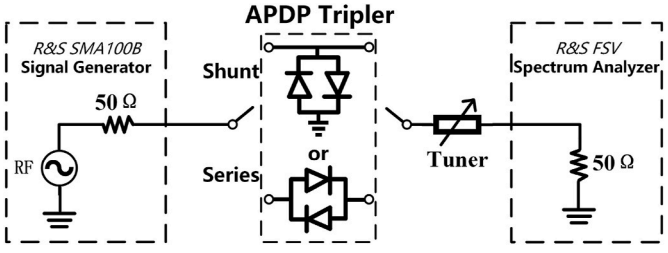

Fig. 2. Measurement setup for two types of APDP triplers.

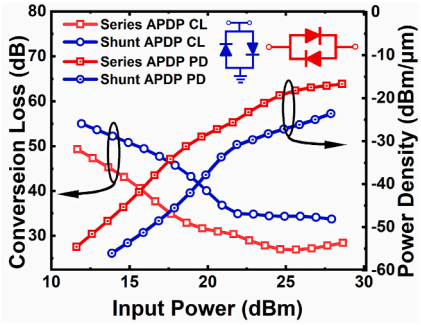

Fig. 3. Output power density and conversion loss versus input power at output frequency of 3.6 GHz.

GaN based APDP. (Since V_{th} of GaN SBD used in this work is relatively larger than those reported in Refs. [13,20,21], and the off-zone of APDP is correspondingly wider). In addition, output PD of series APDP tripler was found always larger than that of shunt APDP at the same input power. It was attributed to the difference of voltage swing on two kinds of APDPs with the same input power. The voltage swing on series APDP was relatively lager than shunt APDP due to the small load impedance (50 Ω standard for spectrum analyzer, shown in Fig. 2) would weaken the voltage swing on shunt connected APDP, while series APDP can capture almost all input power. A large voltage swing would enhance the generation of output power, whereas small voltage swing would worsen the feed through of input signal and result in relatively small output PD in shunt APDP tripler. Overall, to obtain a larger output power at the operating frequency of 3.6 GHz, series APDP tripler would be a preferred choice.

3. Compact model design and verification

Fig. 4(a) and (b) show the compact models of shunt APDP and series APDP on SiC substrate. Parasitic capacitance, resistance, and inductance generated from electrode pads of both types of APDPs were modeled as C_P, R_S, and L_P, respectively. The resistance between channel and substrate was modeled as R_P. For series connected APDP, an extra *trans*-capacitance (C_{ex}) existed between input and output of APDP due to the small interval between electrodes of two SBDs. SBD used in this simulation employed standard nonlinear SPICE diode model in Advanced Design System (ADS), and its classic small signal equivalent circuit is shown in Fig. 4(c). The equivalent circuit consisted of voltage dependent junction capacitance (C_i) and nonlinear current source (I_D), and voltage independent ohmic resistance (R_{on}). C_i and I_D can be written as functions of voltage drop (V_D) on the SBD, which are illustrated in (5) and (6), respectively [22].

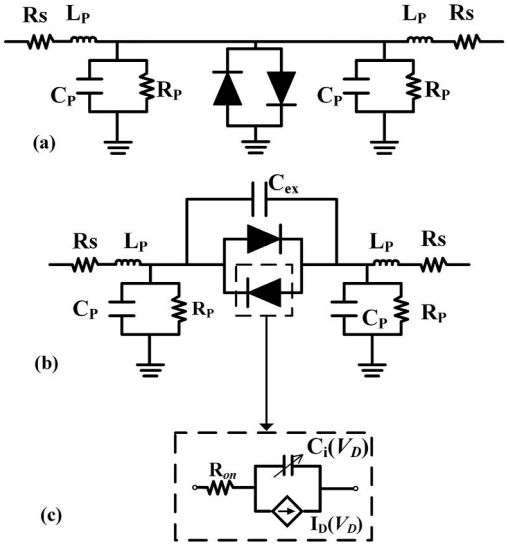

Fig. 4. Large signal compact model for (a). shunt APDP, (b). series APDP, and (c). nonlinear model for SBD.

$$I_D(V_D) = I_S\left(\exp\left(\frac{qV_D - I_D R_{on}}{NkT}\right) - 1\right) \tag{5}$$

$$C_i(V_D) = \frac{C_{i0}}{\left(1 - V_D/V_j\right)^M} \tag{6}$$

where V_j is the junction potential, C_{i0} the junction capacitance at zero bias, and M the grading coefficient. SPICE parameters and parasitic parameters can be extracted precisely by employing I–V curve of APDP and broad band small signal S-parameters measurement. Modeling flows for both of triplers are shown as follows, and all simulations were implemented in ADS.

3.1. Parameters extraction using I–V curve

Fig. 5 illustrates the logarithmic relation of measured I–V curve, as represented in black square scatters. The parameters including N, R_{on}, and I_S can be extracted from the I–V curve. A linear relation between V_D and log (I_D) can be observed at a voltage range of 1 V–1.5 V, approximately. In the method of extracting N and I_S which is reported in Ref. [23], at the linear region, I–V relation can be simplified as (7) due to $V_D \gg kT/q$.

$$I_D = I_S \exp(qV_D / NkT) \tag{7}$$

Hence logarithmic form of I–V relation can be written as:

$$\log(I_D) = \log(I_S) + \frac{qV_D}{2.3NkT} \tag{8}$$

From (8), initial values of N and I_S can be extracted from the slope of log (I_D) versus V_D and axis interpret where $V_D = 0$, respectively. In addition, an optimization in ADS was employed to extract I_S and N more precisely, while R_{on} can be determined in the same time. In this optimization, measured I–V data was imported into ADS as a generic MDIF file, and nominal optimization iterated 2000 times under a bias range of −3 to 3 V. I_S, N, and R_{on} were ultimately determined to be 0.26 μA, 8.94, and 85.58 Ω, respectively. The relatively large N of 8.94 indicated the large threshold voltage of the SBDs, which also enable APDP topology have wide off-zone region to achieve large output power [13]. Fig. 5 compares the measured and simulated I–V characteristic of SBD, and there is an excellent agreement between measurement and simulation.

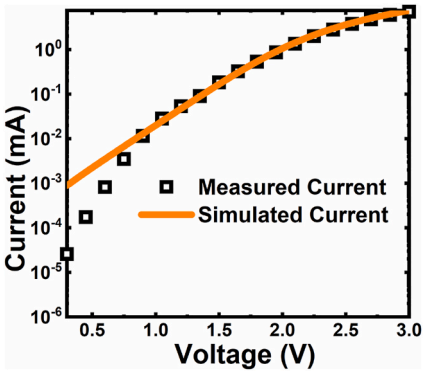

Fig. 5. Simulated and measured I–V characteristic of APDP.

3.2. Power-independent parameters extraction

SBD SPICE parameters of V_j, C_{i0}, and M and parasitic parameters (R_s, R_P, C_P, L_P, and C_{ex}) of APDP can be extracted by on chip broad band S-parameter measurement due to they are power independent. The S-parameter measurement was executed by Keysight Vector Network Analyzer (VNA) at RF power of −20 dBm with 0 V bias, where both SBDs in APDP were not conducting. VNA was calibrated to two probes using Short-Open-Load-Through (SOLT) calibration from 10 MHz to 10 GHz. Then the measured S-parameters were imported into ADS as a touchstone file to fit and optimize the model parameters by using SP simulation. SPICE parameters of C_{i0}, V_j and M were determined to be 820 fF, 0.69 V, and 0.57, respectively. The optimized parasitic parameters for both types of APDP are shown in Table 1.

Fig. 6 shows simulated and measured S_{11} in Smith chart and S_{21} with magnitude and phase for both types of APDPs. S-parameters of S_{22} and S_{12} are not shown in the figure due to $S_{11} = S_{22}$ and $S_{12} = S_{21}$ in the geometrically symmetric APDPs [24]. S_{11} of series connected APDP near the periphery of Smith chart exhibits more resistive than that of shunt APDP. For S_{21}, as increasing frequency, magnitude of S_{21} for series connected APDP showed a rapid increase and then saturated, while the S_{21} magnitude of shunt connected APDP decreased with the increasing frequency. These changes in S_{21} of both types of APDPs were attributed to the increasing feed through in junction capacitance of SBD. Excellent agreement can be observed in all S-parameters between measurement and simulation, which means the APDP compact model can well reflect the device performance.

3.3. Tripler performance verification

After all the parameters were determined by DC and small-signal simulations, the APDP compact models then could work for different input power levels and were used to demonstrate the performance when operated as frequency triplers. In order to simulate the triplers as accurately as possible, influence of input/output coaxial line and the impedance tuner at output of APDP were taken into consideration. Hence the tripler simulation network consisted of three parts. As shown in Fig. 7, the first part was the S-parameters file of input coaxial line, which was connected to the input of compact model. The second part was APDP compact model. The S-parameters file of output coaxial line and impedance tuner composed the third part of tripler simulation network, and they were connected to the output of compact model. Large signal simulation at output frequency of 3.6 GHz was done by using Harmonic Balance (HB) simulation in ADS with an input power range of 10 dBm to 28 dBm.

Fig. 8 plots the comparison between measured and simulated output PD of both types of APDP triplers versus input power. They showed good agreement when input power was larger than 20 dBm, which validated the accuracy of the compact models. Nevertheless, measured output PD of both types of APDP triplers were found to be smaller than the results extracted from simulations when input power was smaller than 20 dBm (At input power of 15 dBm, measured result of series APDP tripler was 7.00 dB smaller than simulated result, while the value for shunt APDP tripler was 4.54 dB). It was attributed to the current mismatch (M_I), defined as the difference-to-sum ratio of the magnitude of currents at two opposite bias voltages [25], between two fabricated SBDs in APDP,

Table 1
Extracted SPICE and parasitic parameters.

Paras.	Series APDP	Shunt APDP
R_S	9.64 Ω	4.54 Ω
R_P	16 MΩ	11 MΩ
C_P	22.96 fF	169 fF
L_P	96 pH	130 pH
C_{ex}	172 fF	N/A

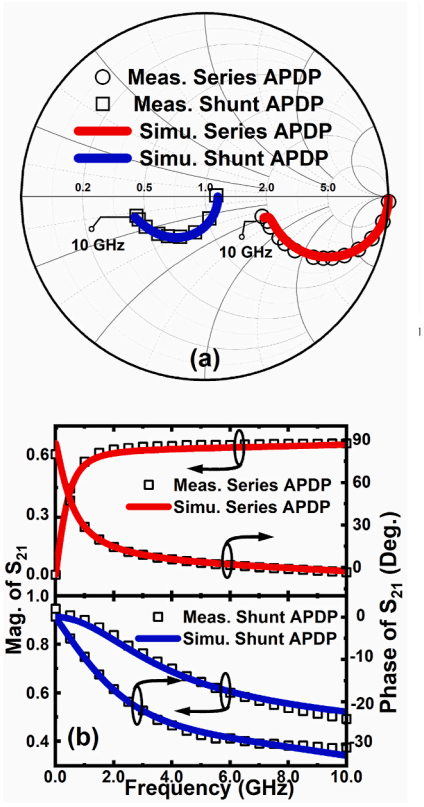

Fig. 6. Simulated and measured small-signal scattering parameters for series connected and shunt connected APDP from 10 MHz to 10 GHz. (a). S_{11} for two types of APDP in Smith Chart view (the Smith chart is normalized at $Z_0 = 50$ Ω), (b) S_{21} for two types of APDP.

which leaded to asymmetric on I–V characteristics of APDP.

Fig. 9 plots the quantified M_I of both types of APDPs versus bias. As increasing the bias, M_I of series APDP and shunt APDP steeply decreased from 85% to 41%, respectively. Both M_I were smaller than 10% when bias was larger than 2 V. Thus, when bias is smaller than 2 V, the generation of output power were seriously weakened due to the relatively large current mismatch [25], which in turn led to the smaller output power in measurement than that of simulated results. When input power was large enough, the mismatch would be as low as 10% for the current at low bias was so small that the M_I can be neglected. The excellent agreement of measurement results and simulation at large input power verifies the precision of the compact models.

Fig. 10 reports 2nd and 4th harmonic suppressions, defined as $\text{supression}|_{Nth}$ (dBc) = $P_{out|Nth}$ (dBm)- P_{in} (dBm), at input frequency of 1.2 GHz versus input power to evaluate the harmonics generation of GaN based series APDP tripler in this work. The 2nd harmonic suppression was typically unchanged with input power, and it was determined to be 18 dBc at input power of 25 dBm. The 4th harmonic (4.8 GHz) suppression decreased as increasing input power. Nevertheless, the smallest 4th harmonic suppression was still as high as 24.86 dBc, which made it possible that no high Q band pass filter (BPF) is in need when designing RFIC. Theoretically, there should have no even harmonics at output of APDP. The observed harmonics of 2.4 GHz and 4.8 GHz were attributed to the mismatch between two SBDs in APDP.

Performances of GaN based APDP frequency triplers are summarized and compared with the previously reported triplers from various technologies in Table 2. Compared with APDP frequency triplers with GaAs and CMOS technologies, the maximum output power of GaN series APDP tripler is much larger than APDP tripler in CMOS technology, and also larger than that of APDP tripler using GaAs SBDs. The triplers in this work also show higher even-order harmonics suppression than those of

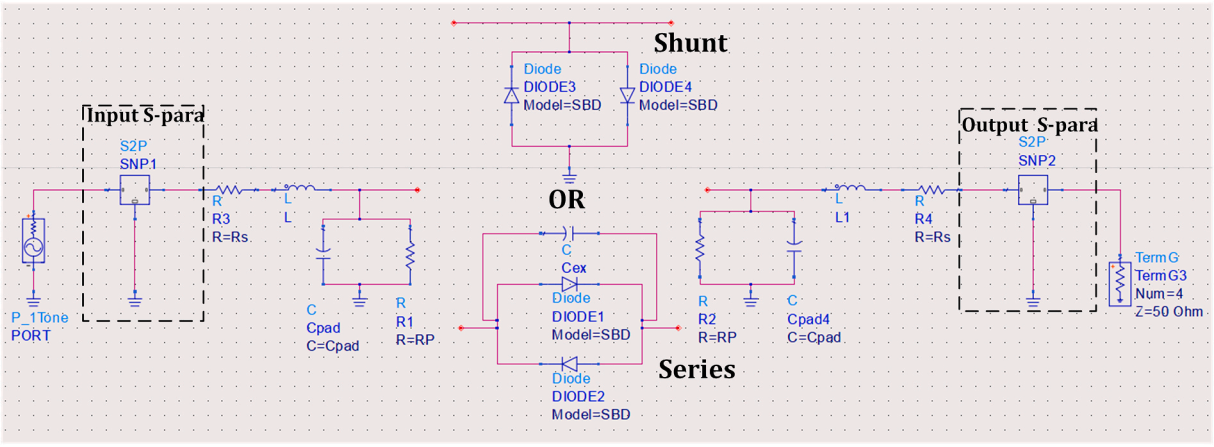

Fig. 7. Simulation setup in ADS.

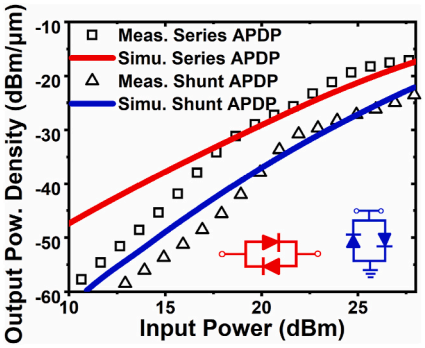

Fig. 8. Simulated and measured output power density of two types of APDP triplers.

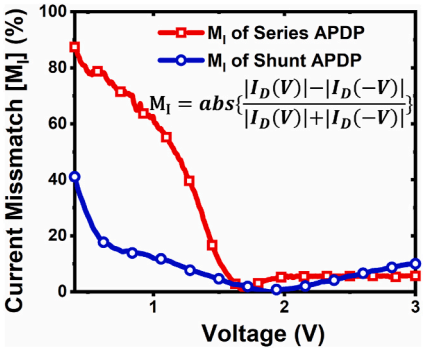

Fig. 9. Measured current mismatch between two diodes in APDP versus bias voltage.

CMOS and GaAs triplers, though there are no band-pass filters or idlers at the output of APDPs. In addition, the triplers in this work are also quite promising when compared to the active triplers shown in Table 2, for the excellent even-order harmonics suppression, large output power, and modest CL with no DC consumption. There is still room of improvement for GaN based APDP tripler. For instance, an idler circuit which could terminate the non-input and non-output signals may be employed to improve CL of the APDP tripler [29,30]. For the constituting GaN SBD, further shrunk channel length and channel resistance are of great interest for higher frequency applications.

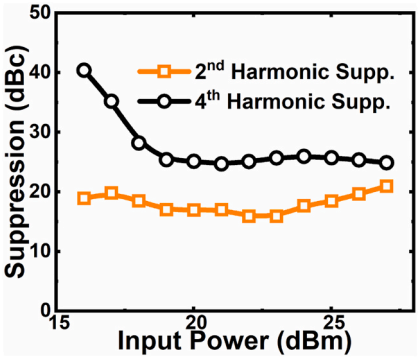

Fig. 10. Suppression for 2nd and 4th harmonics versus input power at input frequency of 1.2 GHz.

4. Conclusion

Based on GaN-on-SiC SBD pair, both series APDP tripler and shunt APDP tripler have been demonstrated and modeled in this study. Series APDP tripler achieved larger maximum output power of −0.14 dBm and smaller minimum CL of 26.9 dB, compared with shunt APDP tripler at an output frequency of 3.6 GHz. It was attributed to the relatively larger voltage swing on series APDP. When being operated with large input power, APDP tripler showed modest current mismatch. Hence, it exhibited 18 dBc suppression for 2nd harmonic with input power of 25 dBm even no BPF was used at the output of the tripler. Furthermore, precise compact models for two types of triplers were proposed. Nonlinear SPICE parameters of SBDs and parasitic parameters of triplers were extracted by DC characteristics and broad band small signal measurements. With a de-embedded tripler network, simulation results computed using the extracted parameters showed excellent agreement with measurement results. Frequency tripler based on GaN APDP and its corresponding model enable precise prediction and effective implementation of high performance frequency triplers with large output power and even harmonics rejection.

Credit author statement

Junmin Zhou: Investigation, Methodology, Formal analysis, Data curation, Writing – original draft, Writing – review & editing, Visualization, **Haowen Guo**: Formal analysis, Writing – review & editing., **Yitian Gu**: Methodology, Discussion., **Xinbo Zou**: Conceptualization, Methodology, Writing – original draft, Writing – review & editing, Validation, Supervision, Project administration, Funding acquisition.

Table 2
Performance summary and comparison with previous reports.

Ref.	Struc.	Output freq. (GHz)	DC pow.	Techn.	Mini. CL (dB)	Pout.max (dBm)	2nd,4th Harm. Supp.[a] (dBc)
This work (series)	GaN APDP	3.6	0	1 μm GaN	26.9	−0.14	21, 25
This work (shunt)					33.7	−6.59	N/A
[26]	N-type varactor Tripler	30	0	45 nm SOI CMOS	24.3	−8	20.1, N/A
[27]	Balanced APDP tripler in GaAs	180	0	0.1 μm GaAs	21	−5	10, N/A
[11]	APDP in Si-CMOS	108	0	22 nm SOI CMOS	38	−16	N/A, 46
[9]	Fund. Cancel Trip.[b]	4.5	43.1 mW	0.18 μm CMOS	39[d]	−15[d]	<-9, 15[d]
[10]	GaN HEMT	11.4	>0[e]	0.5 μm GaN	5.2	19.8	13, N/A
[6]	Injection-locked Trip.[b]	4.8	3.7 mW	0.18 μm CMOS	28[d]	−13	22,30
[28]	Graph. FET	0.3	84.6 μW	CVD Graph.[c]	53.16	N/A	17,15,

a. Measured at the max input power. b. Abbreviation for tripler. c. Chemical vapor deposition Graphene. d. Calculated results due to there is no direct report. e. 15 V on drain and −1.5 V on gate.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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