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Dynamic Characteristics of GaN MISHEMT With 5-nm *In-Situ* SiN_x Dielectric Layer

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ABSTRACT A comprehensive study on dynamic characteristics of GaN MISHEMT with a 5nm-thick *in-situ* SiN_x dielectric is presented. Effects of both negative and positive gate bias on threshold voltage instability were investigated and miniature threshold voltage shift was acquired. The slight shift was considered to be associated with the traps at the insulator/AlGaN interface and in the dielectric layer itself. Pulsed I-V measurements with various gate quiescent biases presented small current collapse (11%) and low enhancement of dynamic R_{on} for zero quiescent drain bias. When drain quiescent bias was strengthened to 20V, an increased dynamic R_{on}/static R_{on} ratio was identified but still limited to a low value of 1.24. The conduction reduction was in a good agreement with measurement results from drain current transient spectroscopy and possibly originates from trap states existed in the access region. Additional current collapse was observed in hard switching-on operation, resulted from energetic hot electrons accelerated by drain-source electrical field during the off-to-on step. The measurement results showed stabilized threshold voltage, a low dynamic R_{on}/static R_{on} ratio, and suppressed current collapse via employing a 5-nm thin *in-situ* SiN_x layer in GaN MISHEMT, enabling it a promising solution for high-efficiency power switching applications.

INDEX TERMS Current collapse, dynamic characteristics, gallium nitride (GaN), *in-situ* SiN_x, metal insulator semiconductor high electron mobility transistors (MISHEMTs), pulsed I-V measurement, threshold voltage instability.

I. INTRODUCTION

AlGaN/GaN-based high electron mobility transistor (HEMT), with high critical electrical field and large carrier mobility, enabled high-performance switching devices for next-generation power conversion applications [1]. Meanwhile, outstanding cut-off frequency and high breakdown voltage offered interesting prospects for radar, wireless communication, RF power amplifiers, and radio astronomy [2], [3]. Compared with conventional HEMT devices, metal-insulator-semiconductor HEMT (MISHEMT) could effectively reduce gate leakage and improve gate modulation ability. Several kinds of dielectrics had been employed as the gate insulator materials in GaN MISHEMT, including Al_2O_3 [4]–[10], HfO_2 [11], [12], HfSiO [13], ZrO_2 [14]–[20], Ga_2O_3 [21], SiO_2 [22], [23], and SiN_x [24]–[34].

Among these gate insulators, SiN_x is one of the most widely-used gate dielectrics, due to its easy access and mutuality in deposition process. At present, GaN MISHEMT with *ex-situ* SiN_x by low-pressure chemical

vapor deposition (LPCVD) had shown good performance in terms of dielectric breakdown [28], [35]. Meanwhile, *in-situ* deposition of SiN_x by metal-organic chemical vapor deposition (MOCVD) on top of the AlGaN/GaN heterostructure was also proposed to mitigate the potential damage and avoid contamination caused by after-growth fabrication process. Lu *et al.* used *in-situ* SiN_x layer as the dielectric for the ultra-thin-barrier AlN/GaN MISHEMTs [36]. The gate leakage of MIS diode was about 7 orders lower than that of Schottky diode. Ma *et al.* fabricated *in-situ* SiN_x/AlN/GaN MISHEMTs with regrown n-GaN source/drain [37]. The device exhibited a gate leakage of below 10^{-4} mA/mm at $V_{gs} = -8$V, leading to a large on/off current ratio over 10^7. Cheng *et al.* deposited a 47nm-thick *in-situ* SiN_x layer as dielectric on AlGaN/GaN heterostructure and realized a efficient leakage suppression with leakage current $< 10^{-8}$ mA/mm [29]. Jiang *et al.* developed a bilayer passivation scheme to fabricate GaN MISHEMTs [32]. A low trap density of $\sim 3 \times 10^{12}$ $cm^{-2}eV^{-1}$ at the SiN_x/AlGaN interface was identified.

There have been some reports on the dynamic performances of GaN MISHEMT with relatively thick *in-situ* SiN_x dielectric. GaN MISHEMT fabricated by a gate-first technology and with a 47nm-thick *in-situ* SiN_x layer exhibited a relatively smaller threshold voltage (V_{th}) shift [27]. The gate-first devices featured a V_{th} shift of -2.03V for a negative gate bias of -30V after a stress period of 10000s, compared with a V_{th} shift of -5.17V for gate-last devices. Tri-field-plate GaN MISHEMT with 50nm *in-situ* SiN_x dielectric showed a small V_{th} shift of less than 0.5V after stressing at $V_{gs} = -35$V and $V_{ds} = 0$V for 1000s [25].

It should also be noted that insertion of a thick *in-situ* SiN_x dielectric in MISHEMT usually required a relatively large reverse bias voltage to turn off the device. It is demanding to have a high-quality thin *in-situ* SiN_x in MISHEMT to simultaneously provide a moderate threshold voltage, low reverse leakage, and outstanding dynamic performance. However, a comprehensive understanding of dynamic characteristics with such a thin dielectric MISHEMT is currently not available.

In this study, an explicit study on dynamic performances of GaN MISHEMT with a 5nm thin *in-situ* SiN_x is reported. Firstly, threshold voltage instabilities of GaN MISHEMT upon various gate biases were investigated. Then current collapse and on-resistance (R_{on}) degradation were assessed by pulsed I-V tests with various quiescent biases. Furthermore, time-resolved drain current (I_{ds}) and R_{on} were also investigated by drain current transient (DCT) spectroscopy. Lastly, the influence of hard switching on output characteristic was demonstrated. With a 5nm *in-situ* SiN_x dielectric, GaN MISHEMT which exhibited excellent V_{th} stability, insignificant increase of dynamic R_{on}, and low current collapse, enabled a promising device technology for high-speed switching applications.

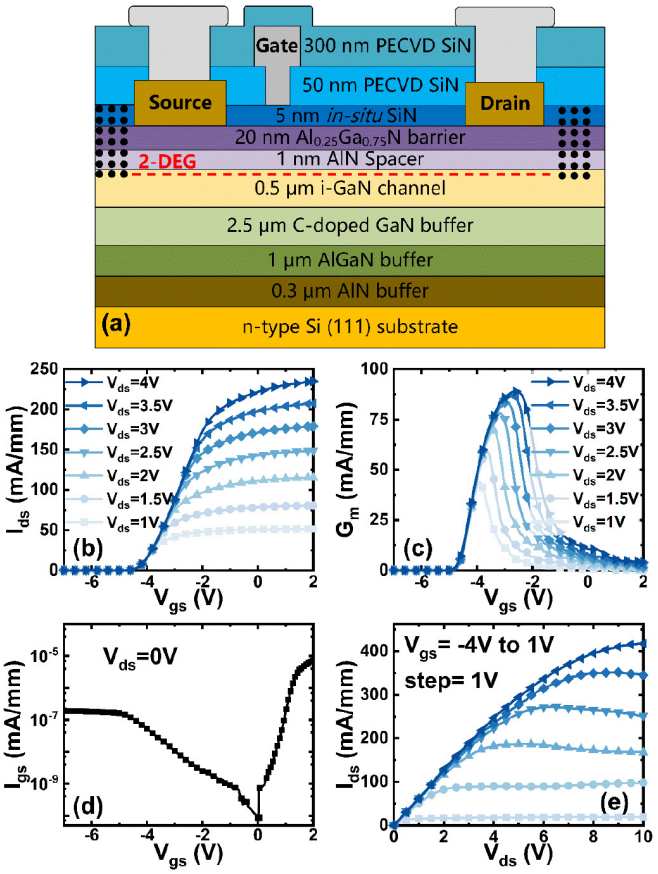

FIGURE 1. (a) Cross-sectional schematic of GaN MISHEMT with 5nm *in-situ* SiN_x. (b) Transfer, (c) transconductance, (d) leakage, and (e) output characteristics.

II. EXPERIMENT AND MEASUREMENT

Fig. 1(a) showed a cross-sectional schematic of AlGaN/GaN MISHEMT with 5nm *in-situ* SiN_x gate dielectric layer. The sample was grown by metal-organic chemical vapor deposition (MOCVD) on 6-inch silicon substrate. The epilayers were composed of a 2.5-μm GaN buffer, a 500-nm unintentionally doped GaN channel layer, a 1-nm AlN spacer, a 20-nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 5-nm thin *in-situ* SiN_x cap. The *in-situ* SiN_x was deposited on top of the AlGaN/GaN heterostructure using silane and ammonia as precursors. The as-grown epilayer showed smooth surface with a root mean square roughness of 0.6 nm across a 5 μm×5 μm scanned area. The X-ray diffraction measurement revealed an average full-width at half-maximum (FWHM) of 526 arcsec for GaN (0002) plane. Device fabrication started with *in-situ* SiN_x removal in the Ohmic contact regions for source/drain metallization. Ohmic contacts were then formed by annealing the Ti/Al/Ni/Au metal stack in N_2 atmosphere. The device isolation was achieved using Ar implantation. A 50-nm SiN_x passivation layer was firstly deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300°C. The PECVD SiN_x layer in the gate region was then removed with a hybrid dry- and wet-etching. The dry etching was performed using

reactive ion etching with SF_6 as the etching gas and the wet etching was performed using HF-based acid. Subsequently, gate metal was deposited using a Ni/Au-based metal stack. Finally, a 300 nm SiN_x layer was deposited by PECVD on the top of the 50 nm SiN_x layer for device passivation. The gate–drain distance L_{gd}, gate–source distance L_{gs}, gate length L_g, and gate width W_g were 15μm, 3μm, 2μm, and 0.4 mm, respectively.

Both electrical static & dynamic properties of *in-situ* SiN_x/AlGaN/GaN MISHEMT, including transfer characteristics, output properties, threshold voltage instability, and pulsed I-V characteristics were measured using semiconductor device analyzer. The principles and waveforms of stress-recovery-measurement, double pulse measurement, and drain current transient measurement with pre-stressing could be found elsewhere [38]–[41].

III. DEVICE RESULTS AND DISCUSSION

Fig. 1(b) showed the transfer characteristics of GaN MISHEMT with a 5 nm *in-situ* SiN_x dielectric layer. The transfer curves revealed V_{th} of −4.5 V defined at I_{ds} of 1 mA/mm, with $V_{ds} = 1V$. The peak transconductance was measured to be 89 mS/mm with $V_{ds} = 4V$, as shown in Fig. 1(c). The device exhibited a low gate leakage current of 1.9×10^{-7} mA/mm at $V_{gs} = -7V$ [Fig. 1(d)]. A high I_{on}/I_{off} ratio of 10^9 and a subthreshold slope (SS) of 125 mV/decade were acquired, indicating excellent gate control capability and switching characteristics of MISHEMT. The output characteristics of the device were illustrated in Fig. 1 (e), showing saturation drain current density of MISHEMT was 417.7 mA/mm at V_{gs} of 1V.

NBTI (negative bias-induced threshold-voltage instability) and PBTI (positive bias-induced threshold-voltage instability) measurements had been employed to study degradation of device characteristics after exposure to gate stressing bias. Fig. 2 displayed NBTI measurement results with various reverse gate bias voltages and durations. As shown in Fig. 2(a), a very small negative shift in V_{th} could be noticed after the device was exposed to a negative gate stress of −7V ($V_{gs,stress} = -7V$) for 200s. In addition to the V_{th} shift, the decrease of the I_{ds} (at $V_{gs} = -1V$ and $V_{ds} = 1V$) could also be observed when $V_{g,stress}$ increased to −10V, as shown in Fig. 2(b). Fig. 2(c)–(d) illustrated that the offset of V_{th} was further expanded for the device with $V_{gs,stress} = -15V$ and $V_{gs,stress} = -20V$. Meanwhile, compared with the results in the condition of $V_{gs,stress} = -7V$, I_{ds} (at $V_{gs} = -1V$ and $V_{ds} = 1V$) was also further reduced given by the same stressing duration.

Fig. 2(e) showed transfer curves after stressing at various gate biases for the same stressing duration of 200s. When the device was exposed to a higher $V_{gs,stress}$, a relatively larger positive V_{th} shift was observed. Fig. 2(f) summarized V_{th} shift and I_{ds} reduction ratio (at $V_{gs} = -1V$ and $V_{ds} = 1V$) as a function of the reverse gate bias. When a harsh stressing condition was applied ($V_{gs,stress} = -20V$ for 200s), ΔV_{th} was measured to be 0.11 V, suggesting the device with 5-nm

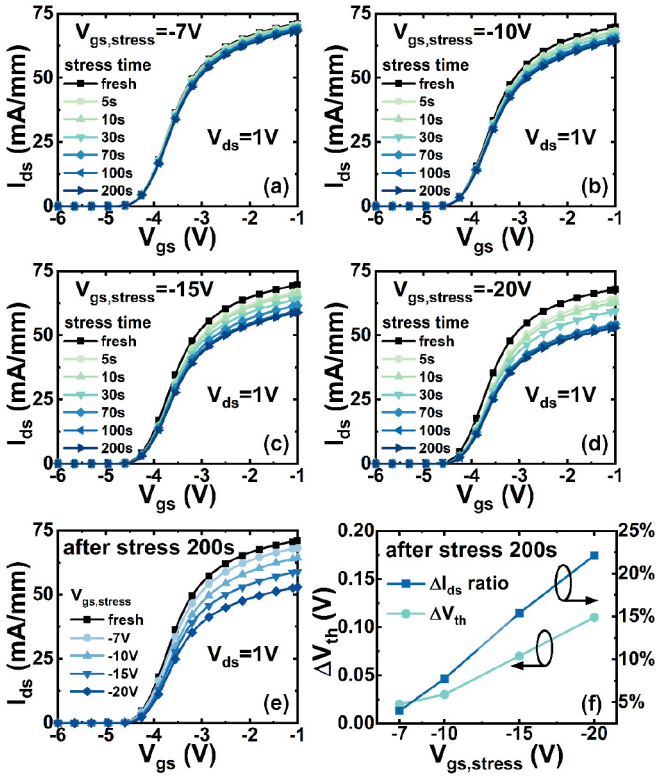

FIGURE 2. **(a)-(d) NBTI performances after various reverse gate bias and stressing durations. (e) I_{ds}-V_{gs} curves after stressing at negative gate biases of −7V, −10V, −15V, and −20V for 200s. (f) V_{th} shift and I_{ds} reduction ratio at $V_{gs} = -1V$.**

thin *in-situ* SiN_x dielectric had excellent V_{th} stability. On the other hand, a drain current drop could be observed after different $V_{gs,stress}$ condition. The drain current was reduced by 22% upon −20V gate stressing ($V_{gs,stress} = -20V$) for 200s.

The positive shift of V_{th} was related to trap states in the gate dielectric and at the insulator/AlGaN interface. These trap states would capture electrons injected from gate when the gate was applied with negative stress voltage ($V_{gs,stress} < V_{th}$). Thus, trapped electrons in the dielectric and at the dielectric/AlGaN interface repelled the 2DEG in the channel and drove the V_{th} shift positively as well as decreased the drain current. The shift of V_{th} was also related to the magnitude of $V_{gs,stress}$ [Fig. 2(e)]. With the same stressing time, a larger $V_{gs,stress}$ would enhance the electrons injection from the gate, leading to relatively larger V_{th} shift and reduction of I_{ds}, as summarized in Fig. 2 (f).

Fig. 3 showed V_{th} variation and I_{ds} drop (measured at $V_{gs} = -1V$ and $V_{ds} = 1V$) as a function of recovery time in the recovery process ($V_{gs} = 0V$, $V_{ds} = 0V$). The recovery process of the device was followed by a pre-stressing step, which differed in pre-stressing gate voltages from −7V to −20V, but all with a stressing duration of 200s. In the recovery process, the gate and drain were all biased to 0V.

As shown in Fig. 3(a), it was noticed that the V_{th} gradually moved towards non-stressed fresh state ($\Delta V_{th} = 0V$) as the extension of recovery time. The results revealed that captured electrons in the dielectric and at the dielectric/AlGaN

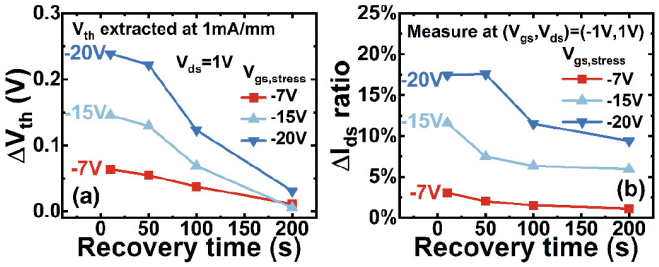

FIGURE 3. Variation of (a) threshold voltage and (b) drain current at $V_{gs} = -1V$ after negative gate stress 200s at different biases.

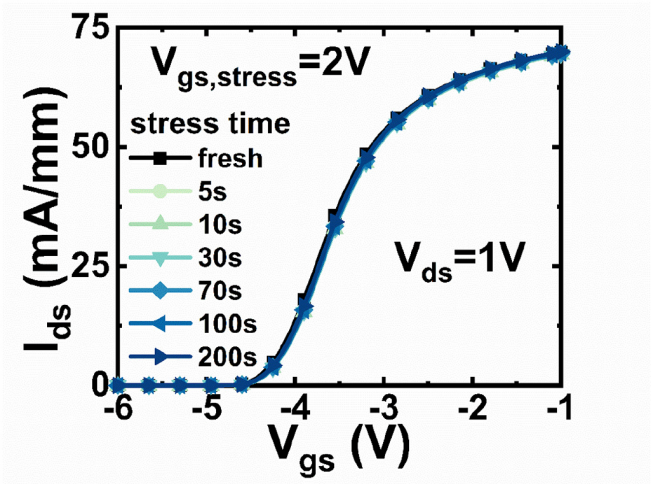

FIGURE 4. PBTI measurement results after $V_{gs,stress} = 2V$ for different stress durations.

interface would be released gradually once the device recovered naturally without any bias applied (V_{gs} = 0V, V_{ds} = 0V). The device with 200s recovery time almost recovered to the fresh state after pre-stressing at −7V and −15V. In the case of pre-stressing at −20V, there was still a small ΔV_{th} after 200s-recovery, indicating the V_{th} needed even longer rest time to restore completely. The result showed that a longer recovery time was required for GaN MISHEMT to return to the initial state if a larger pre-stress voltage was applied.

With pre-stress at $V_{gs,stress} = -7V$, I_{ds} almost got replenished to its initial value after 200s-recovery, as shown in Fig. 3 (b). In addition, it should also be noted that in the case of $V_{gs,stress} = -15V$ and −20V, I_{ds} did not fully recover to its initial value when V_{th} had reached its original value of fresh state after 200s recovery. This phenomenon was associated with enhanced carrier capture effect in the access region with a relatively high $V_{gs,stress}$. Some slow trap states in the access region further reduced the drain current and exhibited a longer recovery time for I_{ds}.

Fig. 4 showed transfer curve measurement results upon positive gate bias stressing ($V_{gs,stress} = +2V$) at room temperature. As the positive stressing duration was extended from 5s to 200s, negligible V_{th} was observed. Compared with NBTI measurement, GaN MISHEMT could maintain

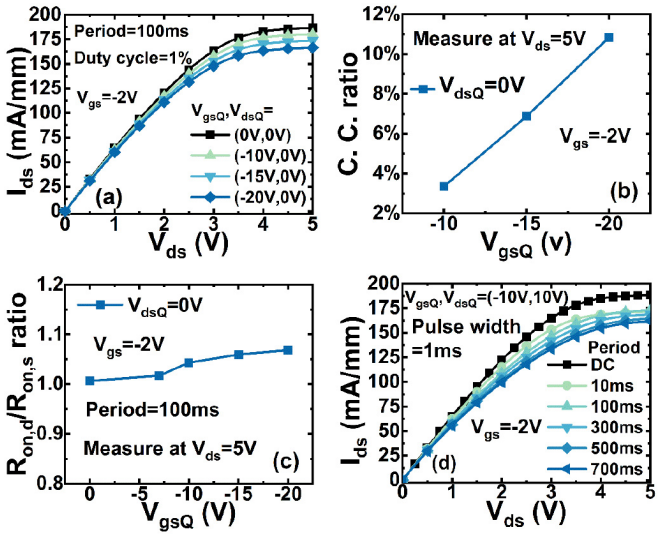

FIGURE 5. (a) Pulsed I_{ds}–V_{ds} performance of GaN MISHEMT with different V_{gsQ} ($V_{gs} = -2V$ and $V_{dsQ} = 0V$). (b) Current collapse and (c) $R_{on,d}/R_{on,s}$ ratio. (d) Pulsed I_{ds}–V_{ds} performance of GaN MISHEMT with different periods ($V_{gsQ} = -10V$ and $V_{dsQ} = 10V$).

steady V_{th} and reliable forward conduction after positive gate bias stressing.

Pulsed I-V measurements were carried out to reveal the current collapse (C. C.) behavior in the GaN MISHEMT. Fig. 5(a) showed pulsed I-V characteristics of the device with various quiescent gate voltages (V_{gsQ}) while retaining the zero quiescent drain voltage (V_{dsQ}). In this measurement, pulse width and pulse period were set to be 1ms and 100ms, respectively, to assure that sufficient electrons were captured in the off-state stressing and the on-state measurement itself had little impact on the device performance. Current collapse ratio was evaluated as the decrease of I_{ds} at V_{ds} = 5V and increase of R_{on} was defined as the dynamic R_{on}/static R_{on} ($R_{on,d}/R_{on,s}$) ratio, where $R_{on,s}$ was measured at non-stressing condition [(V_{gsQ}, V_{dsQ}) = (0V, 0V)]. When the device was biased at the $V_{gsQ} = -10V$, a negligible current collapse ratio of 3.6% was observed and current reduction was slightly worsened with increasing the V_{gsQ}.

Fig. 5(b)-(c) showed the extracted current collapse ratio and $R_{on,d}/R_{on,s}$ ratio of the GaN MISHEMT with different V_{gsQ}. The current collapse ratio was increased to 11% as the V_{gsQ} was strengthened to −20V. However, there was minor variation of R_{on} as increasing the V_{gsQ} from −7V to −20V. This phenomenon was consistent with the observation of Fig. 2 (a)-(d). The V_{th} and I_{ds} exhibited a small variation with short stress time (<5s). It was also found that current collapse was highly dependent on the stressing period of pulsed IV tests. As shown in Fig. 5(d), worsened current collapse could be observed with prolonging period from 10ms to 100ms.

Fig. 6 showed the pulsed output characteristics of GaN MISHEMT with various quiescent biases. Fig. 6(a) illustrated dependence of current collapse on the

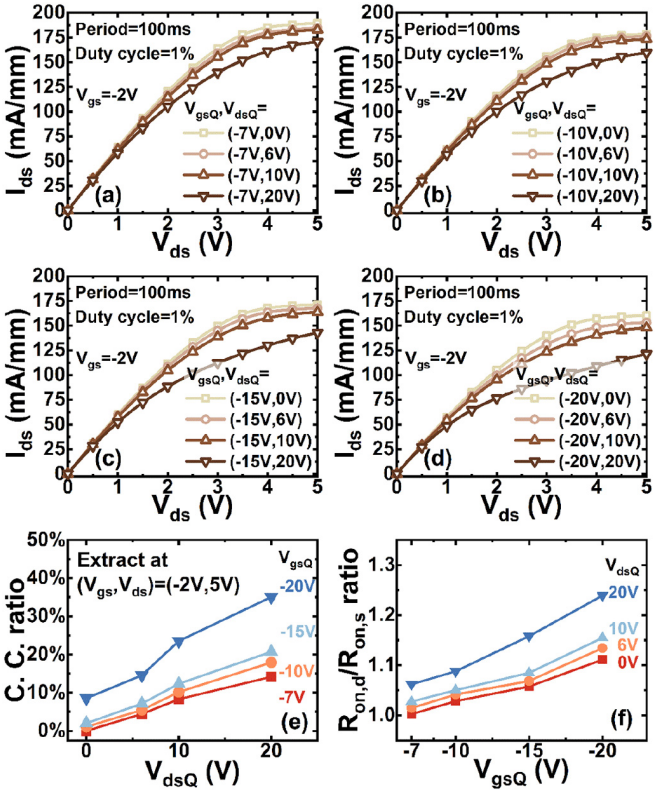

FIGURE 6. (a)-(d) Pulsed I_{ds}–V_{ds} characteristics of the GaN MISHEMT with various quiescent biases. (e) Current collapse and (f) $R_{on,d}/R_{on,s}$ ratio.

TABLE 1. $R_{on,d}/R_{on,s}$ performance comparison of MISHEMT with 5nm *in-situ* SiN_x and other dielectrics in the literature.

Ref.	Dielectric	Thickness (nm)	V_{gsQ},V_{dsQ}	$R_{on,d}/R_{on,s}$	W_g (μm)
This work	*in-situ* SiN_x	5	(-20V, 20V)	1.24	400
[31]	LPCVD Si_3N_4	30	(-18V, 40V)	2.00*	10
[28]	*in-situ* + LPCVD Si_3N_4	33	(-14V, 600V)	1.34	N.A.
[42]	AlN	20	(-8V, 50V)	2.30	50
[13]	HfSiO	15	(0V, 600V)	1.17	50

*Estimated value

quiescent drain bias with fixed V_{gsQ} of −7V. Compared with the case of V_{dsQ} = 0V, the dynamic degradation at higher V_{dsQ}, as illustrated as increase of dynamic R_{on}, were promoted due to the exacerbation of charge trapping in the access region, which occurred simultaneously with the surface charge trapping. As shown in Fig. 6(a)-(d), the current collapse was also related to the magnitude of $V_{gs,stress}$. With the same V_{dsQ}, a relatively larger I_{ds} degradation was spotted with a lager pre-set V_{gsQ}.

Fig. 6 (e)-(f) illustrated extracted current collapse and $R_{on,d}/R_{on,s}$ ratio as a function of the quiescent gate bias with different V_{dsQ}. The current collapse ratio exhibited a monotonic increase with V_{dsQ} at a pre-set V_{gsQ}. The current collapse reached 35% at V_{gsQ} = −20V and V_{dsQ} = 20V [Fig. 6 (e)]. Conventional Schottky-gate HEMTs have been reported that considerable current collapse (>80%) may occur at room temperature [39], [40], [43]. Compared with conventional Schottky-gate HEMT, MISHEMT with a 5nm *in-situ* SiN_x dielectric layer could endure lager stressing condition and significantly improve current collapse. As shown in Fig. 6 (f), $R_{on,d}/R_{on,s}$ ratio was also slightly increased as V_{dsQ} was strengthened. $R_{on,d}/R_{on,s}$ ratio was still limited to a low value of 1.24, although the device was quiescently biased with V_{dsQ} of 20V and V_{gsQ} of −20V. In the recent literatures, the GaN MISHEMT with relative thick dielectrics [*in-situ* + LPCVD Si_3N_4 (33nm)] had achieved effective dynamic R_{on} suppression [28]. A high-*k* dielectric 15nm HfSiO together with a field-plate scheme was developed to reduce dynamic R_{on} under a large V_{dsQ} condition [13]. In addition, adoption of thick AlN (20nm) or LPCVD-Si_3N_4 (30nm) dielectric well suppressed the increase of dynamic R_{on} ($R_{on,d}/R_{on,s}$ ratio is about 2) in the case of V_{gsQ} near V_{th} and V_{dsQ} was set as dozens of volts [31], [42]. In this work, a low $R_{on,d}/R_{on,s}$ ratio of 1.24 has been achieved based on a thin and high quality *in-situ* SiN_x layer, when being stressed with relative large gate and drain bias: V_{gsQ} = −20V (15V below V_{th}) and V_{dsQ} = 20V.

DCT measurement was employed to illustrate time-resolved conduction of GaN MISHEMT. By applying a semi-continuous stressing bias on the device, drain current transient spectrum could be acquired by probing the device repeatedly. Fig. 7(a) displayed normalized I_{ds} as a function of stressing time. The dynamic I_{ds} was measured in the linear region (V_{gs} = −2V and V_{ds} = 0.2V) when the device was switched to on-state. The normalized I_{ds} was defined as the ($I_{ds,dynamic}/I_{ds,static}$), where $I_{ds,static}$ was measured in the non-stressed fresh state [(V_{gs}, V_{ds}) = (−2V, 0.2V)]. From time-dependent measurements, the drain current did not change until the device was exposed to the off-state stressing for 100ms, and gradually decreased afterwards due to accumulation of trapped carrier. Fig. 7(b) showed normalized R_{on} ratio as a function of stressing duration. The normalized R_{on} was defined as the $R_{on,d}/R_{on,s}$. A gently increased normalized R_{on} ratio was observed as extending the stressing time. The insignificant change of R_{on} suggested good surface passivation by thin *in-situ* SiN_x.

Fig. 8 depicted output characteristics of GaN MISHEMT with drain-to-gate delay (DGD) from 4 μs to −4 μs and quiescent bias of (V_{gsQ}, V_{dsQ}) = (−7V, 10V). DGD was defined as the time difference between V_{ds} = (V_{ds_on} + V_{ds_off})/2 and V_{gs} = V_{th}. The DGD became positive in the case of a soft-switching mode, while it was negative with a hard-switching operation. For soft-switching condition (DGD > 0), the current collapse showed a DGD-irrelevant performance with different DGD values. However, the current collapse was worsened in the hard-switching condition (DGD < 0). And the saturation current showed a steady reduction with DGD = −4μs, compared with soft-switching. This additional current collapse was associated with high energy electrons [38], [39], [44]. During hard-switching, the

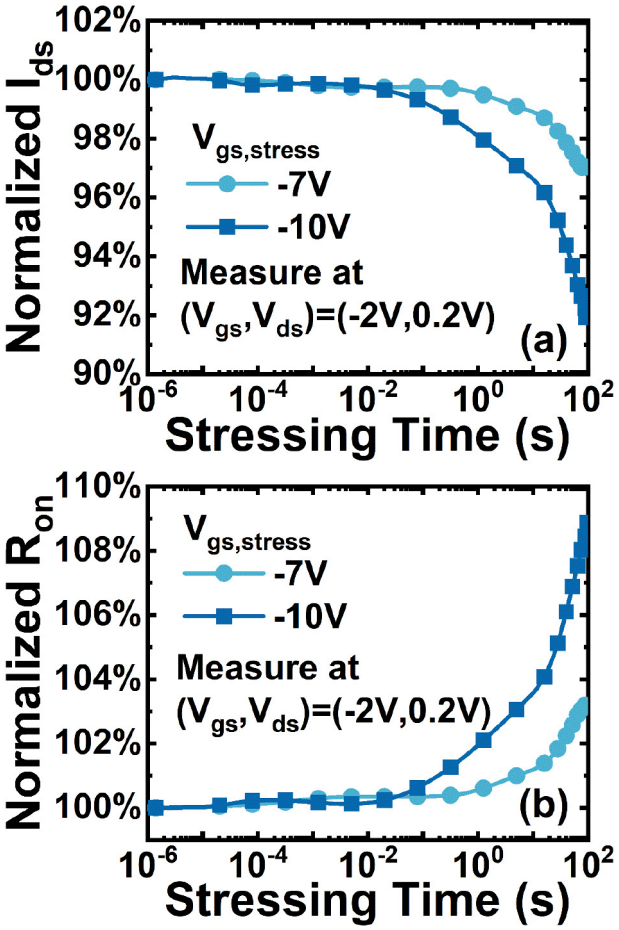

FIGURE 7. (a)-(b) Time-resolved I_{ds} and R_{on} for $V_{gs,stress}$ of −7V and −10V.

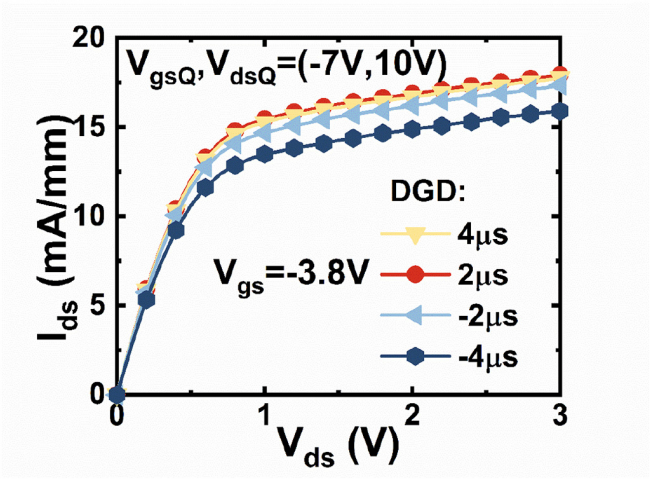

FIGURE 8. Pulsed I_{ds}−V_{ds} characteristics of the GaN MISHEMTs with (V_{gsQ}, V_{dsQ}) = (−7V, 10V) for various drain-to-gate delays.

device was in large drain bias condition when V_{gs} crossed the threshold voltage, resulting in the generation of high energy electrons. Accelerated high energy electrons in large drain bias condition would aid additional carrier trapping in the AlGaN or in the buffer.

IV. CONCLUSION

In conclusion, the dynamic characteristics of GaN MISHEMT with a 5nm-thick *in-situ* SiN_x dielectric was quantitatively investigated. Transfer characteristics measurements after various gate stressing conditions had been carried out to reveal threshold voltage instability. The threshold voltage was shifted by 0.11V in the case of the device was stressed at a reverse gate bias of −20V for 200s, illustrating high threshold voltage stability of MISHEMT with a 5-nm thin *in-situ* SiN_x dielectric layer. Moreover, pulsed I-V measurement results showed that 11% current collapse was observed by applying negative gate bias stressing only. However, current collapse was significantly enhanced to 35%, together with a degraded R_{on}, when applying a combination of relative large gate and drain bias: $V_{gsQ} = -20V$ and $V_{dsQ} = 20V$. The large lateral electric field formed in the access region would accelerate the electron trapping process, thus leading to a worsened dynamic performance. Drain current transient measurement also exhibited a reduced forward current and increased R_{on}, as extending stressing time, in a good agreement with NBTI measurement results. Compared with soft switching-on mode, it was also observed that hard switching-on operation would cause extra current collapse, resulted from energetic hot electrons accelerated by large drain-source electrical field during the switching process.

REFERENCES

[1] M. Meneghini *et al.*, "GaN-based power devices: Physics, reliability, and perspectives," *J. Appl. Phys.*, vol. 130, no. 18, 2021, Art. no. 181101.
[2] A. S. A. Fletcher and D. Nirmal, "A survey of Gallium Nitride HEMT for RF and high power applications," *Superlattices Microstruct.*, vol. 109, pp. 519–537, Sep. 2017.
[3] M. Ťapajna, "Current understanding of bias-temperature instabilities in GaN MIS transistors for power switching applications," *Crystals*, vol. 10, no. 12, p. 1153, 2020.
[4] V. Putcha *et al.*, "Exploring the DC reliability metrics for scaled GaN-on-Si devices targeted for RF/5G applications," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2020, pp. 1–8.
[5] M. Tao *et al.*, "Characterization of 880 V normally off GaN MOSHEMT on silicon substrate fabricated with a plasma-free, self-terminated gate recess process," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1453–1457, Apr. 2018.
[6] J. Gao *et al.*, "Gate-recessed normally OFF GaN MOSHEMT with high-temperature oxidation/wet etching using LPCVD Si_3N_4 as the mask," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1728–1733, May 2018.
[7] Y. K. Lin *et al.*, "High-performance GaN MOSHEMTs fabricated with ALD Al_2O_3 dielectric and NBE gate recess technology for high frequency power applications," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 771–774, Jun. 2017.
[8] F. Sang *et al.*, "Time-dependent threshold voltage drift induced by interface traps in normally-off GaN MOSFET with different gate recess technique," *Appl. Phys. Exp.*, vol. 9, no. 9, 2016, Art. no. 91001.
[9] Y. Shi, W. Chen, Z. Fu, S. Chen, and B. Zhang, "Influence of the acceptor-type trap on the threshold voltage of the short-channel GaN MOS-HEMT," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 606–611, 2021.
[10] H. Wang *et al.*, "AlGaN/GaN MIS-HEMTs with high quality ALD-Al_2O_3 gate dielectric using water and remote oxygen plasma as oxidants," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 110–115, 2018.

[11] H. Chandrasekar *et al.*, "Dielectric engineering of HfO_2 gate-stacks for normally-ON GaN HEMTs on 200-mm silicon substrates," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3711–3718, Sep. 2018.
[12] Y. T. Shi *et al.*, "High-*k*HfO_2-based AlGaN/GaN MIS-HEMTs With Y_2O_3 interfacial layer for high gate controllability and interface quality," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 15–19, 2020.
[13] Q. Hu *et al.*, "Improved current collapse in recessed AlGaN/GaN MOS-HEMTs by interface and structure engineering," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4591–4596, Nov. 2019.
[14] P. Cui *et al.*, "InAlN/GaN metal–insulator–semiconductor high-electron-mobility transistor with plasma enhanced atomic layer-deposited ZrO_2 as gate dielectric," *Jpn. J. Appl. Phys.*, vol. 59, no. 2, 2020, Art. no. 20901.
[15] H. Jiang, C. W. Tang, and K. M. Lau, "Enhancement-mode GaN MOS-HEMTs with recess-free barrier engineering and high-*k* ZrO_2 gate dielectric," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 405–408, Mar. 2018.
[16] H. Jiang, C. Liu, K. W. Ng, C. W. Tang, and K. M. Lau, "High-performance AlGaN/GaN/Si power MOSHEMTs with ZrO_2 gate dielectric," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5337–5342, Dec. 2018.
[17] Y.-C. Byun *et al.*, "Low temperature (100 °C) atomic layer deposited-ZrO_2 for recessed gate GaN HEMTs on Si," *Appl. Phys. Lett.*, vol. 111, no. 8, 2017, Art. no. 82905.
[18] T. J. Anderson *et al.*, "Enhancement mode AlGaN/GaN MOS high-electron-mobility transistors with ZrO_2 gate dielectric deposited by atomic layer deposition," *Appl. Phys. Exp.*, vol. 9, no. 7, 2016, Art. no. 71003.
[19] R. Stoklas, D. Gregušová, K. Hušeková, J. Marek, and P. Kordoš, "Trapped charge effects in AlGaN/GaN metal-oxide-semiconductor structures with Al_2O_3 and ZrO_2 gate insulator," *Semicond. Sci. Technol.*, vol. 29, no. 4, 2014, Art. no. 45003.
[20] M. Hatano, Y. Taniguchi, S. Kodama, H. Tokuda, and M. Kuzuhara, "Reduced gate leakage and high thermal stability of AlGaN/GaN MIS-HEMTs using ZrO_2/Al_2O_3 gate dielectric stack," *Appl. Phys. Exp.*, vol. 7, no. 4, 2014, Art. no. 44101.
[21] H. Y. Lee, T. W. Chang, E. Y. Chang, N. Rorsman, and C. T. Lee, "Fabrication and characterization of GaN-based fin-channel array metal-oxide-semiconductor high-electron mobility transistors with recessed-gate and Ga2O3 gate insulator layer," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 393–399, 2021.
[22] A. Chakroun *et al.*, "AlGaN/GaN MOS-HEMT device fabricated using a high quality PECVD passivation process," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 779–782, Jun. 2017.
[23] F. Husna, M. Lachab, M. Sultana, V. Adivarahan, Q. Fareed, and A. Khan, "High-temperature performance of AlGaN/GaN MOSHEMT with SiO_2 gate insulator fabricated on Si (111) substrate," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2424–2429, Sep. 2012.
[24] H. Wang *et al.*, "1.3 kV reverse-blocking AlGaN/GaN MISHEMT with ultralow turn-on voltage 0.25 V," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 125–129, 2021.
[25] F. Li *et al.*, "Temperature-dependent hot electron effects and degradation mechanisms in 650-V GaN-based MIS-HEMT power devices under hard switching operations," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6424–6431, Oct. 2021.
[26] Q. Zhu *et al.*, "Negative bias-induced threshold voltage instability and zener/interface trapping mechanism in GaN-based MIS-HEMTs," *Chin. Phys. B*, vol. 29, no. 4, 2020, Art. no. 47304.
[27] L. Cheng *et al.*, "Gate-first AlGaN/GaN HEMT technology for enhanced threshold voltage stability based on MOCVD-grown *in situ* SiN_x," *J. Phys. D, Appl. Phys.*, vol. 54, no. 1, 2020, Art. no. 15105.
[28] H. Sun *et al.*, "Investigation of the trap states and V_{TH} instability in LPCVD Si_3N_4/AlGaN/GaN MIS-HEMTs with an *in-situ* Si_3N_4 interfacial layer," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3290–3295, Aug. 2019.
[29] L. Cheng *et al.*, "Gate-first process compatible, high-quality *in situ* SiN_X for surface passivation and gate dielectrics in AlGaN/GaN MISHEMTs," *J. Phys. D, Appl. Phys.*, vol. 52, no. 30, 2019, Art. no. 305105.
[30] S. Warnock, A. Lemus, J. Joh, S. Krishnan, S. Pendharkar, and J. A. D. Alamo, "Time-dependent dielectric breakdown in high-voltage GaN MIS-HEMTs: The role of temperature," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3132–3138, Aug. 2017.
[31] X. Lu, K. Yu, H. Jiang, A. Zhang, and K. M. Lau, "Study of interface traps in AlGaN/GaN MISHEMTs using LPCVD SiN_x as gate dielectric," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 824–831, Mar. 2017.
[32] H. Jiang, C. Liu, Y. Chen, X. Lu, C. W. Tang, and K. M. Lau, "Investigation of *In Situ* SiN as gate dielectric and surface passivation for GaN MISHEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 832–839, Mar. 2017.
[33] H. Chiu *et al.*, "RF performance of *In Situ* SiN_x Gate Dielectric AlGaN/GaN MISHEMT on 6-in silicon-on-insulator substrate," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4065–4070, Oct. 2017.
[34] H. Wang, F. J. Lumbantoruan, T. Hsieh, C. Wu, Y. Lin, and E. Y. Chang, "High-performance LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs With 850-V 0.98-m$\Omega\cdot cm^2$ for power device applications," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1136–1141, 2018.
[35] M. Hua *et al.*, "Normally-off LPCVD-SiN_x/GaN MIS-FET with crystalline oxidation interlayer," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 929–932, Jul. 2017.
[36] X. Lu, J. Ma, Z. Liu, H. Jiang, T. Huang, and K. M. Lau, "In situ SiN_x gate dielectric by MOCVD for low-leakage-current ultra-thin-barrier AlN/GaN MISHEMTs on Si," *Physica Status Solidi A*, vol. 211, no. 4, pp. 775–778, 2014.
[37] J. Ma *et al.*, "MOVPE growth of *in situ* SiN_x/AlN/GaN MISHEMTs with low leakage current and high on/off current ratio," *J. Cryst. Growth*, vol. 414, pp. 237–242, Mar. 2015.
[38] Y. Wang *et al.*, "Comparative study on dynamic characteristics of GaN HEMT at 300K and 150K," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 850–856, 2020.
[39] Y. Gu, Y. Wang, J. Chen, B. Chen, M. Wang, and X. Zou, "Temperature-dependent dynamic degradation of carbon-doped GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3290–3295, Jul. 2021.
[40] V. Nagarajan *et al.*, "Study of charge trapping effects on AlGaN/GaN HEMTs under UV illumination with pulsed I-V measurement," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 2, pp. 436–441, Jun. 2020.
[41] X. Zhou *et al.*, "Dynamic characteristics of AlGaN/GaN Fin-MISHEMTs with Al_2O_3 dielectric," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 928–935, Mar. 2018.
[42] J.-J. Zhu *et al.*, "Improved interface and transport properties of AlGaN/GaN MIS-HEMTs with PEALD-grown AlN gate dielectric," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 512–518, Feb. 2015.
[43] A. K. Visvkarma *et al.*, "Impact of gamma radiations on static, pulsed *I-V*, and RF performance parameters of AlGaN/GaN HEMT," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2299–2306, May 2022.
[44] Y. Gu *et al.*, "Temperature-dependent dynamic performance of p-GaN Gate HEMT on Si," *IEEE Trans. Electron Devices*, vol. 69, no. 6, pp. 3302–3309, Jun. 2022.