Dynamic Reliability Assessment of Vertical GaN Trench MOSFETs with Thick Bottom Dielectric

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***Abstract*—Dynamic stability of quasi-vertical GaN trench MOSFETs featuring a thick bottom dielectric (TBD) is thoroughly investigated. Degradation in forward drain current was observed as applying gate or drain stressing voltage, and further studied by time-resolved measurements. The drain current of the device can be maintained at 79%, compared to 61% of a reference device without TBD. Meanwhile, repeated switching tests conducted within a short on-state time demonstrate that the current collapse is confined to 10% after 500 switching cycles. The current collapse is related to electron capture at the dielectric/GaN interface, and the introduction of TBD reduces the electric field within the dielectric layer and suppresses the capture process of traps. Positive gate bias-induced threshold instability of the device with and without TBD is investigated. For the device with TBD, a small positive threshold voltage shift of 1 V is obtained. In addition, the effect of drain stressing voltage on devices is also revealed. High-resolution drain current transient spectroscopy displays the drain current reduction, attributing the degradation to captured electrons in the n^--GaN layer. A capture activation energy of 0.26 eV is revealed by deep level transient spectroscopy. These findings reveal the efficacy of TBD inclusion in improving gate stability of GaN MOSFETs and underscore the critical importance of high-quality epitaxial growth for ensuring the stability of vertical devices. The stability characterization serves as a valuable reference for the development of reliable quasi-vertical GaN MOSFET devices.**

***Index Terms*—GaN, dynamic characteristics, vertical trench MOSFET**

I. INTRODUCTION

GAN is considered as a promising candidate for next generation high voltage and high power electronic devices, due to its superb material properties, including wide bandgap, high breakdown electric field, high mobility, and high electron saturation drift velocity [1, 2]. Vertical GaN devices have been attracting extensive attention as vertical structure provides efficient current spreading and improved voltage blocking capability. A high breakdown voltage can be achieved by increasing the drift layer thickness, without expanding the footprints of the devices. This feature makes them well-suited for high power applications, such as power electronics and grid-tied inverters. In addition, uniform distribution of the electric field throughout the vertical structure mitigates the surface state issue of the lateral device counterpart, which can alleviate the degradation in dynamic on-resistance and current collapse.

Recently, various types of vertical GaN MOSFETs have been fabricated and reported, including the current aperture vertical electron transistor (CAVET) [3-6], vertical fin MOSFETs [7-11], and vertical trench MOSFETs [12-22]. However, gate opening for the trench structure may induce defects, leading to high-density surface charges that can damage the on-state behavior and dynamic performance of devices. To address this issue, interface engineering and gate stack optimization are recommended to suppress surface traps. A low average interface trap density of GaN surface was found by piranha cleaning [23, 24]. Vertical trench MOSFETs were fabricated on bulk GaN substrates using *in-situ* Al_2O_3 dielectric and GaN interlayer [18]. The device achieved a high breakdown field of 1.6 MV/cm without edge termination. Vertical GaN trench MOSFETs with an on-current of more than 1 A and a breakdown voltage of 485 V have been fabricated and reported by simultaneous piranha cleaning and thick bottom dielectric (TBD) [14, 15].

In addition, some studies have been conducted on the dynamic performance of GaN trench MOSFETs. Improvement of dynamic R_{on} in trench MOSFETs was achieved using a combination of the Reactive Ion Etching (RIE) dry etch and the tetramethylammonium hydroxide (TMAH) wet etch [19]. With this process combination, the dynamic R_{on} was reduced by over 10 times for the same drain stressing voltage. In a separate study, MOSFETs with a bilayer of Al_2O_3 and GaN exhibited a 30% lower switching loss compared to MOSFETs with Al_2O_3 only [20]. An improved breakdown robustness of the GaN vertical MOSFETs with a bilayer insulator (Al_2O_3 and SiO_2) was also revealed [25]. Additionally, the positive bias-induced threshold voltage instability (PBTI) of GaN trench MOSFETs in the high-

This work was supported by ShanghaiTech University Startup Fund 2017F0203-000-14, the National Natural Science Foundation of China (Grant No. 52131303), Natural Science Foundation of Shanghai (Grant No. 22ZR1442300), and in part by CAS Strategic Science and Technology Program under Grant No. XDA18000000. (Corresponding Authors: Xinbo Zou; Kei May Lau.)

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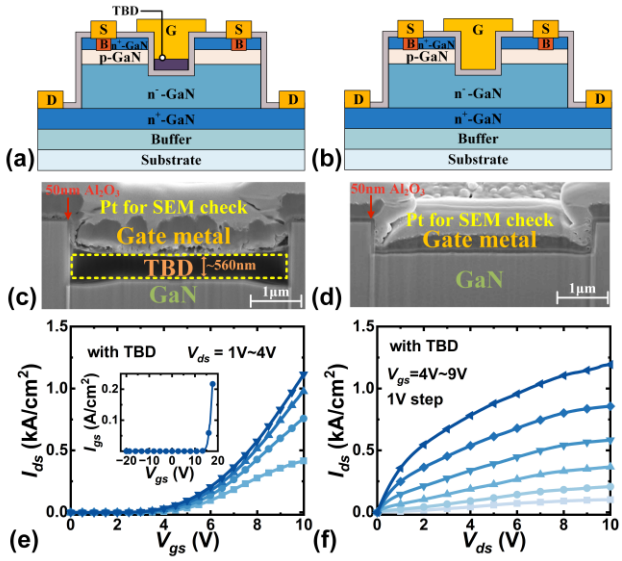

Fig. 1. (a) Cross-sectional schematics of fabricated quasi-vertical GaN trench MOSFET (a) with and (b) without TBD. Cross-sectional SEM images of the gate trench region of devices (c) with TBD and (d) without TBD. The yellow dashed box refers to the TBD. (e) Transfer (inset: gate leakage) and (f) output characteristics of vertical MOSFET with TBD.

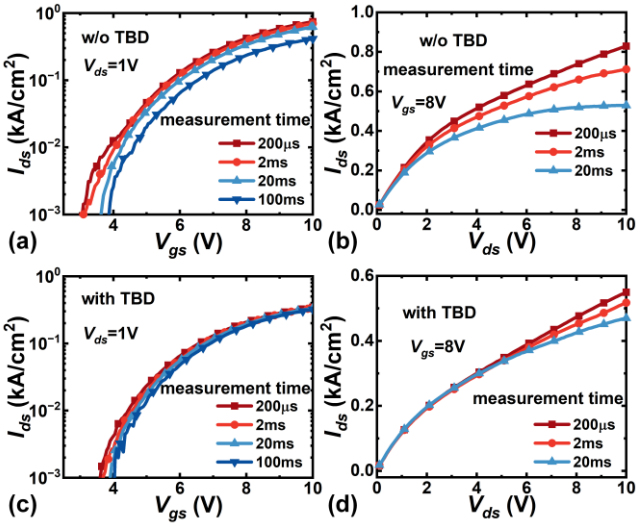

Fig. 2. Transfer characteristics of vertical MOSFET (a) without and (c) with TBD for different measurement times. Output characteristics of vertical MOSFET (b) without and (d) with TBD for different measurement times.

temperature regime was also investigated [26]. A non-monotonic recovery transient was discovered.

Despite the fact that DC performance and gate instability of GaN vertical MOSFET has been documented, time-resolved dynamic behaviors and the impact of drain stressing voltage on the conduction performance of MOSFET have not been thoroughly investigated. Additionally, improved DC performance has been reported by inserting a TBD. However, a comprehensive understanding on gate stability of such a trench device is currently still missing.

In this work, a comprehensive study on the dynamic characteristics of GaN quasi-vertical trench MOSFETs with TBD is reported. The influence of gate and drain voltages on quasi-vertical MOSFETs with and without TBD is investigated through DC test with varying measurement durations. The variation of drain current (I_{ds}) is analyzed through time-resolved I_{ds} from off-state to on-state with various base durations. The degradation of I_{ds} during the repeated switching cycles is also revealed. Threshold voltage (V_{th}) instabilities of MOSFETs upon gate stressing voltage ($V_{gs,stress}$) is characterized by PBTI test. In addition, pulsed output curve and drain current transient spectroscopy (DCTs) are performed to extract the variation of I_{ds} with drain stressing voltage. The shift of V_{th} with various drain stressing voltages is also displayed. Related trap properties are studied by deep level transient spectroscopy (DLTS). The results indicate that quasi-vertical GaN MOSFET with TBD is favorable for improving gate stability. The insight gained from drain instability can be used to optimize the stability of GaN quasi-vertical trench MOSFET devices.

II. Fabrication

Fig.1 (a) displays a cross-sectional schematic of the quasi-vertical trench GaN MOSFETs with thick bottom dielectric. The n+-p-n−-n+-GaN structures were grown by metal organic chemical vapor deposition (MOCVD) on sapphire substrates. The epilayer consisted of a 1-μm i-GaN buffer, a 1-μm n^+-GaN [Si: 5×10^{18} cm^{-3}], a 2.5-μm n^--GaN drift layer [Si: 5×10^{16} cm^{-3}], a 400-nm p-GaN body [Mg: 2.3×10^{19} cm^{-3}], and a 200-nm n^+-GaN layer [Si: 5×10^{18} cm^{-3}] from bottom to top. The fabrication process has been reported in our previous work [15]. A 50-nm Al_2O_3 gate was deposited as dielectric using atomic layer deposition (ALD). To establish the bottom dielectric layer, a layer of ethylene octene copolymer (EOC) was uniformly coated. The EOC has a dielectric constant of 3.6, a breakdown field of 4.1 MV/cm, and a glass transition temperature of 230 ℃. The filling process was followed by curing at 150 ℃ for 30 minutes on a hotplate. Subsequently, a selective etching procedure using O_2 plasma was employed to remove excess EOC material, leaving a thickness of approximately 560 nm EOC exclusively within the gate trench. In our previous work, the influence of TBD thickness on the device has been reported [15]. When the thickness of TBD was increased, the peak electric field at the bottom of the trench decreased, and the breakdown voltage and BFOM increase. The breakdown voltage and BFOM tended to saturate as the TBD thickness continues to increase above 500 nm. Therefore, in this work, the TBD thickness is chosen to be ~560 nm. In addition, as shown in Fig.1 (b), a trench MOSFET that shares the same fabrication process, except TBD, was used to compare dynamic characteristics of MOSFETs with TBD. After device fabrication, the gate stack of the devices with and without TBD were characterized using scanning electron microscopy (SEM), as shown in Fig. 1 (c) and (d). The yellow dashed box refers to the TBD. The devices featured a rectangular gate trench with a 2 μm × 100 μm area. The active area of the device for specific on-resistance and current density normalization is calculated as (2 μm trench length +2.5 μm drift region thickness) × (100 μm

trench width +2.5 μm drift region thickness) = 461.25 μm^2, considering the lateral current spreading length (2.5 μm) in the drift region.

III. Discussion and Results

Fig. 1 (e) shows the transfer characteristics of the quasi-vertical trench GaN MOSFETs with TBD. The V_{th} is determined as 3.5 V, which is defined as the I_{ds} reaching 1 A/cm^2. The fabricated device exhibits a subthreshold swing (SS) of 0.78 V/dec. Additionally, a gate leakage of 1×10^{-7} A/cm^2 can be observed at V_{gs} = -20 V, as shown in the inset of Fig. 1 (e). Fig. 1 (f) illustrates the output curves of the device. A high I_{ds} density of 1.2 kA/cm^2 is obtained at V_{gs} = 9 V and V_{ds} = 10 V. The $R_{on,sp}$ calculated from the linear region is 2.8 mΩ·cm^2.

A. Degradation Induced by On-state Setting

Fig.2 (a) illustrates the transfer characteristics of the GaN vertical MOSFET without TBD under various measurement times. The measurement time refers to the total duration of the DC sweep. As the measurement time is prolonged, V_{th} of the device displays a positive shift. A larger V_{th} shift (ΔV_{th}) of 0.75 V is observed as the measurement time is extended to 100 ms. In addition, the increase of the measurement time also contributes to the current collapse, as shown in Fig.2 (b). A 36% current collapse can be achieved with a measurement time of 20 ms (compared to I_{ds} at 200 μs). Fig.2 (c) – (d) show the transfer and output characteristics of the device with TBD. The device with TBD exhibits a lower shift of V_{th} at the same measurement time compared to the device without TBD. When the measurement time is extended to 100 ms, the V_{th} of the device only shifts by 0.35 V. Meanwhile, the output I_{ds} at measurement time of 20 ms still remain 86 % of initial value (I_{ds} extracted at 200 μs), as shown in Fig.2 (d). These results indicate that the devices are affected by the voltage stressing, including gate and drain stressing voltage during the on-state duration. The device with TBD exhibits more stable performance due to the effective reduction of the electric field by TBD [15], thus suppressing the trapping effect in the gate region. A thick oxide layer on the bottom of the gate trench has also been employed in vertical SiC MOSFET for relieving the electric field strength of the gate oxide layer [27, 28]. Similarly, the enhancement of I_{ds} density and a decrease in on-resistance were observed in vertical GaN MOSFET by the insertion of an MOCVD-regrown GaN interlayer between the n-p-n trenched structure and the dielectric [22].

Fig.3 displays the variation of the I_{ds} of the devices in the on-state process. Fig.3 (a) shows the waveform of short-term time-resolved measurement, including the gate stressing stage and the on-state. An initial drain current ($I_{ds,fresh}$) is measured before the gate stressing stage. The gate stressing voltage is [(V_{gs}, V_{ds}) = (6 V, 0 V)]. During the device switches from gate stressing stage to the on-state [(V_{gs}, V_{ds}) = (8 V, 5 V)], $I_{ds,dynamic}$ is extracted at various time points. The normalized I_{ds} is defined as $I_{ds,dynamic}$ / $I_{ds,fresh}$. The measurement duration of stressing stage and on-state are defined as base time (t_{base}) and on-state time (t_{on}), respectively. As shown in Fig.3 (b), the I_{ds} decreases

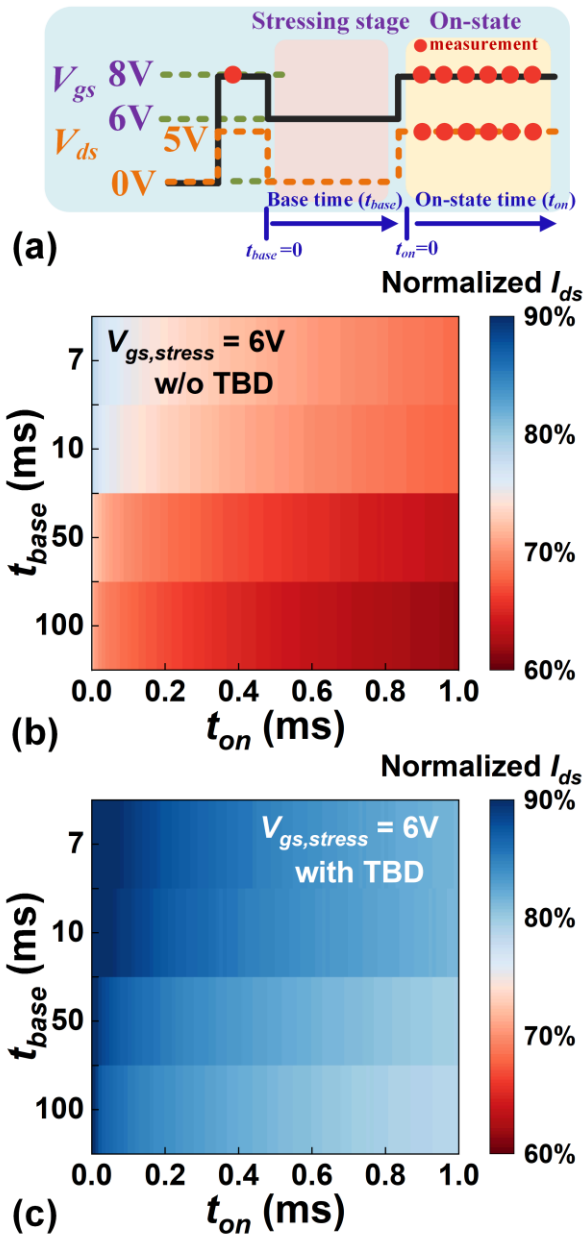

Fig. 3. (a) The waveform of short-term time-resolved measurement. The variation in I_{ds} of the device (b) without and (c) with TBD as a function of t_{on} with various t_{base} at $V_{gs,stress}$ = 6V.

by 20 % after the device is exposed to a $V_{gs,stress}$ of 6 V for 7 ms. I_{ds} will further decline with longer t_{base} and t_{on}. When the t_{base} is increased to 100 ms, the current degradation increases to 39% for a t_{on} of 1 ms. However, the I_{ds} degrades inconspicuously after the device with TBD is subjected to the same $V_{gs,stress}$ for 7 ms and 10 ms, as shown in Fig.3 (c). As the t_{base} increases to 100 ms, only a small current degradation of 5% is observed. The device with TBD displays a current degradation of 21% after maintaining the operating voltage for 1 ms. The results verify the degradation of conduction characteristics during on-state duration. This degradation is related to the operating voltage during on-state duration, as the forward gate and drain

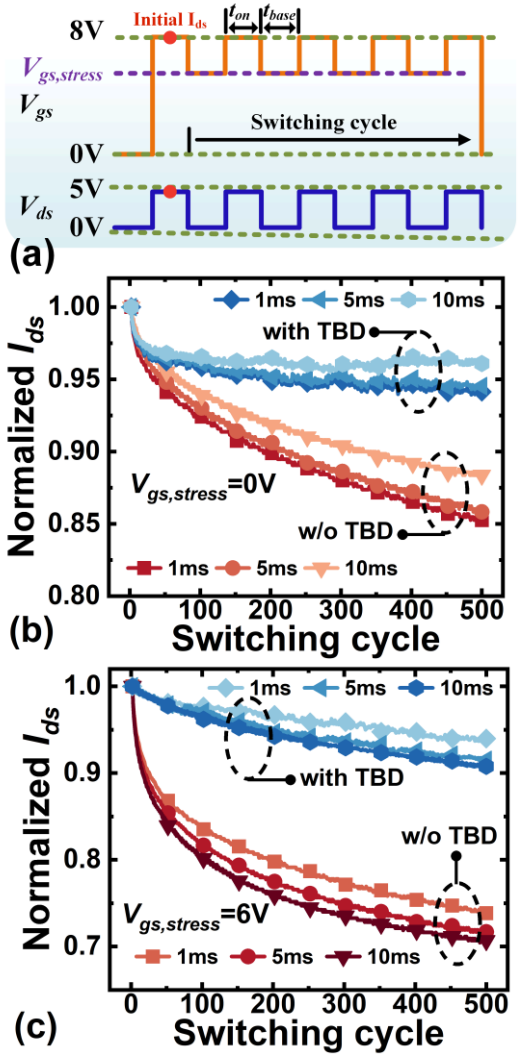

Fig. 4. (a) The waveform of repeated switching measurement. The variation in I_{ds} as a function of switching cycle with various t_{base} at $V_{gs,stress}$ of (b) 0 V and (c) 6 V.

voltages imposed stress on the device. A longer t_{on} and t_{base} will lead to severer degradation of device performance. The faster degradation rate of the devices in the on-state indicates that the combined effect of gate and drain stress accelerates the degradation of the device.

Fig.4 shows the variation in I_{ds} of the device with and without TBD during the repeated switching process. Fig.4 (a) displays the waveform of repeated switching measurement. As shown in Fig.4 (b), after 500 switching repetitions, the device without TBD demonstrates a 15% reduction in I_{ds}, given a t_{base} of 1ms and a $V_{gs,stress}$ of 0V. As the t_{base} increases, the I_{ds} degradation gradually diminishes. The introduction of TBD into the device leads to a decrease in I_{ds} degradation from 15% to 6% at a t_{base} of 1 ms. When the t_{base} is extended to 10 ms, the I_{ds} degradation is only 4% after 500 switching repetitions. As shown in Fig.4 (c), when the $V_{gs,stress}$ is increased to 6 V, the I_{ds} of the device without TBD decreases by 26% for a t_{base} of 1 ms. An increase in t_{base} results in a more pronounced decrease in I_{ds}. The device with TBD exhibits a minor I_{ds} degradation of 6% when t_{base} is

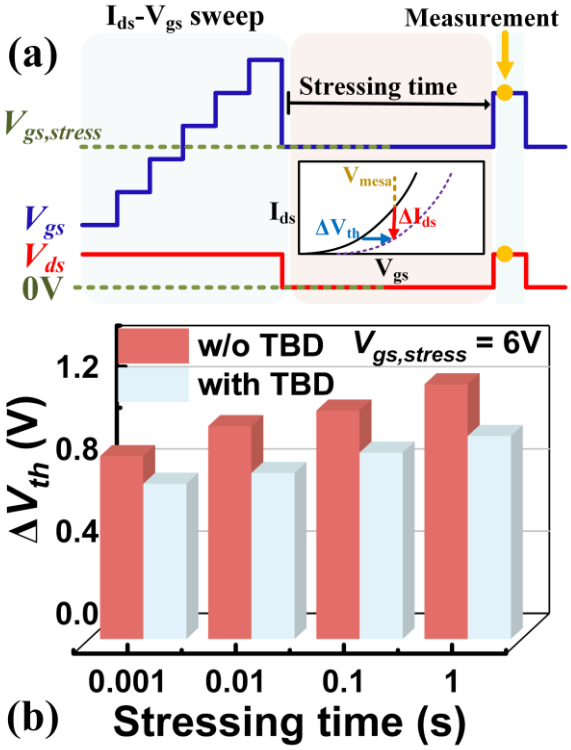

Fig. 5. (a) The V_{th} instability test waveform. (b) ΔV_{th} of the MOSFET with and without TBD at a $V_{gs,stress}$ of 6V.

set to 1 ms. Even if the t_{base} is extended to 10 ms, the I_{ds} degradation remains within 10%.

This phenomenon of I_{ds} degradation in repeated switching is principally attributed to the effect of on-state stressing voltage. When the device is in the on-state, the I_{ds} decreases (as also mentioned in Fig.3). Then the device gradually recovers during the stressing process with a $V_{gs,stress}$ of 0V, resulting in a smaller degradation of I_{ds} as the t_{base} increases [Fig.4 (b)]. However, when a positive $V_{gs,stress}$ is applied, the device continues to degrade during the stressing stage, a more noticeable I_{ds} degradation is found with a longer t_{base} [Fig.4 (c)]. This additional degradation is associated with interface traps of the dielectric layer. When a positive gate stressing is applied to the device, electrons in the conductive channel are captured by interface traps, leading to a decrease in I_{ds}. Compared with the device without TBD, the device with TBD effectively relieves the electric field strength of interface at the corner of the gate trench, thus suppressing the electric field-dependent trapping effect. Therefore, the device with TBD exhibits improved gate stability.

B. Degradation Induced by $V_{gs,stress}$ / $V_{ds,stress}$

Fig.5 shows the time-dependent variation of the V_{th} at a $V_{gs,stress}$ of 6 V. The V_{th} instability is evaluated through Measure-Stress-Measure tests, the tests waveform is shown in Fig.5 (a). This measurement technique consists of an initial I_{ds}–V_{gs} sweep, a stressing process, and a measurement process. The measurement point is (V_{gs}, V_{ds}) = (4 V, 1 V). The I_{ds} data recorded during the measurement process is converted to ΔV_{th}

by the initial I_{ds}–V_{gs}, as shown in the inset of Fig. 5 (a). As shown in Fig. 5 (b), when the MOSFETs are subjected to a positive $V_{gs,stress}$, a positive V_{th} shift can be observed. A ΔV_{th} of 0.9 V is extracted in MOSFET without TBD for a stressing time of 1ms. When the stressing time is extended to 1s, the ΔV_{th} increases to 1.2 V. Compared with the MOSFET without TBD, the MOSFET with TBD exhibits a lower ΔV_{th} of 0.75 V for 1ms. ΔV_{th} only increases to 0.98 V as the stressing time is prolonged to 1s. The positive shift in V_{th} has also been reported in GaN quasi-vertical MOSFETs with some other representative dielectrics. A MOSFET with a bilayer insulator (including 2.5-nm Al_2O_3 and 35-nm SiO_2) achieved a V_{th} shift of about 1.25 V with a positive $V_{gs,stress}$ of 3 V [25]. A trench MOSFET with 35-nm Al_2O_3 showed a ΔV_{th} of 1.2 V extracted by double pulsed test under a $V_{gs,stress}$ of 6 V [29]. In this work, the device with a 50-nm Al_2O_3 dielectric and TBD displays a lower ΔV_{th} of 0.9 V. These results indicate that this device has good V_{th} stability with gate trench treatment and TBD. The positive shift of V_{th} is related to trap states in the gate dielectric and at the dielectric/GaN interface. These trap states will capture electrons when the gate is applied with positive stressing voltage. Captured electrons reduce electron concentration and contribute to a positive shift of V_{th}.

Fig.6 shows the pulsed *I-V* characteristics of the quasi-vertical device with TBD for various drain stressing voltages ($V_{ds,stress}$). During the measurement, the device is repeatedly switched between the testing stage and the drain stressing stage. The bias condition of the testing stage is (V_{gs}, V_{ds}) = (8 V, 5 V). The drain stressing voltages range from 4V to 8V. As shown in Fig.6 (a), when the device is subjected to a $V_{ds,stress}$, a reduced I_{ds} can be observed. A current collapse of 16% is extracted for a $V_{ds,stress}$ of 4 V at a period time of 500 ns and a pulse width time of 1 ms. The current collapse exhibits an escalating trend with increasing $V_{ds,stress}$, reaching 44% at an enhanced $V_{ds,stress}$ of 8 V. Fig.6 (b) displays the pulsed *I-V* performed over a longer period time of 5ms. The current collapse increased to 20% with the same $V_{ds,stress}$ of 4 V. When the $V_{ds,stress}$ is increased to 8 V, a current collapse of 48% is obtained. These results indicate the $V_{ds,stress}$ also contributes to the degradation of device conduction characteristics. The degradation observed in this measurement is mainly caused by $V_{ds,stress}$ due to the much shorter pulse width of 500 ns. The reduction of I_{ds} is related to the electron trapping in the n^--GaN layer. Biasing a forward voltage on the drain terminal of the device (gate voltage is 0 V) is equivalent to applying a reverse voltage to the PIN structure. Thus, the space charge region is increased and electrons are captured by traps in the n^--GaN layer, resulting in a decrease in current. A higher $V_{ds,stress}$ widens the space charge region, leading to an increase in captured electrons and a larger current collapse. Additionally, a longer period time for applying $V_{ds,stress}$ results in an augmented current collapse. Compared with the device without TBD, no additional treatment is applied to the drain region or epilayer of the device with TBD. The instability of the device with TBD is only studied in the case of the drain stressing.

Fig.7 shows the drain current transient spectroscopy of the

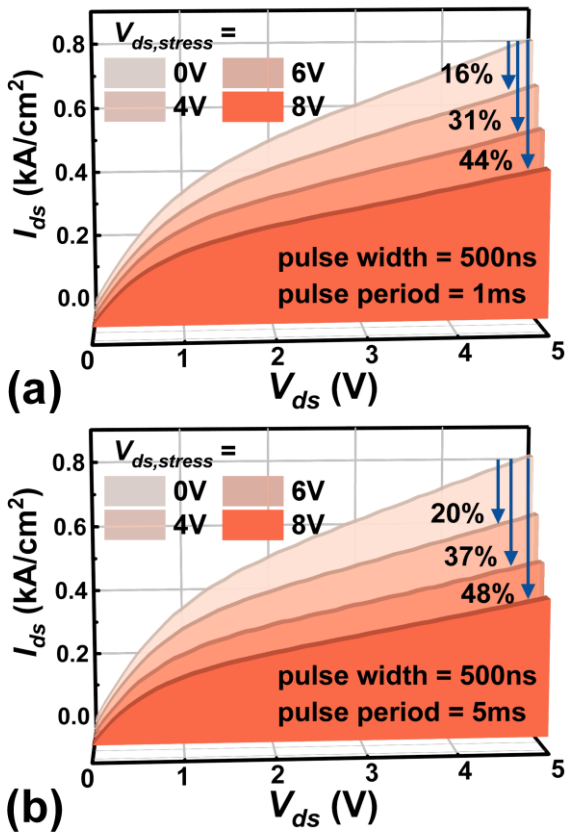

Fig. 6. Pulsed I_{ds}–V_{ds} characteristics of GaN MOSFET with TBD under different $V_{ds,stress}$ for pulse width of 500 ns and pulse period of (a) 1 ms and (b) 5 ms.

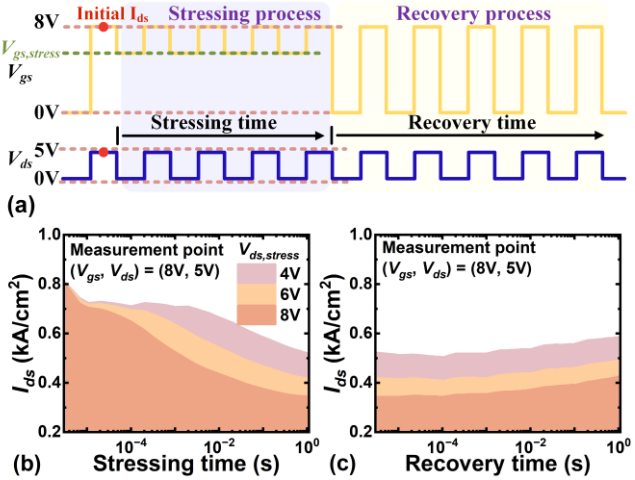

Fig. 7. (a) The drain current transient measurement waveform. The variation in I_{ds} of the device with TBD at various $V_{ds,stress}$ during (b) stressing and (c) recovery process.

device with TBD at different $V_{ds,stress}$. Fig.7 (a) shows the drain current transient measurement waveform. The measurement consists of stressing and recovery process. Fig.7 (b) displays the I_{ds} as a function of stressing time at a fixed measurement point of (V_{gs}, V_{ds}) = (8 V, 5 V). As the stressing time is extended, the I_{ds} decreases due to the capture of electrons by trap states in the

n^--GaN layer. I_{ds} reduces to 36% for a stressing time of 1 s and a $V_{ds,stress}$ of 4 V. The decrease of I_{ds} is accelerated with a relatively higher $V_{ds,stress}$. When the $V_{ds,stress}$ is 8 V for 1 s, the current collapse enhances to 57.6%. Fig.7 (c) shows the variation of I_{ds} during the recovery process after the device is exposed to a stressing time of 1 s. The devices repeatedly switch between the recovery state and the on-state. The bias condition of the recovery state is (V_{gs}, V_{ds}) = (0 V, 0 V). Recovery time refers to the time the device is in the recovery process. During the recovery process, a slow recovery velocity is observed. After the device naturally recovers for 1 s, the I_{ds} does not returns to the initial state. The time-resolved I_{ds} verifies the decrease of I_{ds} during the drain stressing process. When a relatively higher $V_{ds,stress}$ is biased to the device, a quicker degradation is observed. However, slow recovery velocity is also discovered, which indicates the related traps exhibit a longer recovery time constant. A long period of time is required to restore the device to its initial state after being exposed $V_{ds,stress}$.

Fig.8 shows the variation of V_{th} in the device with TBD as a function of stressing time under various positive $V_{ds,stress}$ conditions ($V_{gs,stress}$ = 0 V). When the device is biased to a positive drain stressing voltage, V_{th} shifts to the positive direction. A ΔV_{th} of 0.07 V can be obtained with a $V_{ds,stress}$ of 2 V for a stressing time of 1 ms. With a stressing time of 1 s, a ΔV_{th} of 0.38 V is extracted. A larger ΔV_{th} is observed with increasing $V_{ds,stress}$ at the same stressing time. When $V_{ds,stress}$ is enhanced to 6 V, a ΔV_{th} of 0.52 V is displayed for a stressing time of 1 ms, and ΔV_{th} increases to 1.34 when the stressing time is extended to 1 s. This positive shift of V_{th} is associated with the degradation of I_{ds}. I_{ds} is reduced when the device is exposed to a positive $V_{ds,stress}$. During the stressing process, the traps in the n^--GaN will capture the carriers, contributing to the reduction of I_{ds} and the positive shift of V_{th}.

Fig.9 shows the results of temperature-scanning DLTS measurement conducted on the quasi-vertical GaN MOSFET with TBD. The measurement is performed on the source and drain terminal of device, the gate terminal is floated. The tested structure can be regarded as a PIN structure, where the body electrode contacts the p-GaN. Biasing a reverse voltage U_R of -10 V on source terminal is equivalent to applying drain stressing voltage to the device. Filling pulse U_P, filling pulse width t_P, and measurement period T_W are set to 1 V, 1 ms, and 500 ms, respectively. As shown in Fig.9 (a), DLTS signal reveals a majority carrier trap named E1 at 210 K. Fig.9 (b) displays the Arrhenius plot of E1 obtained from DLTS spectra. From the Arrhenius analysis, the activation energy E_A can be extracted to be 0.26 eV. This majority carrier trap energy is also reported in our previous study of GaN PIN diode [30]. The traps probably originate from nitrogen vacancies generated in the GaN epitaxial growth process [31]. Due to the much higher doping concentration in the p-GaN layer compared to the n^--GaN layer, the space charge region is primarily located in the n^--GaN layer, suggesting that the traps are mainly distributed in the n^--GaN layer. Consequently, electrons can be captured in the traps when the device is exposed to the positive $V_{ds,stress}$,

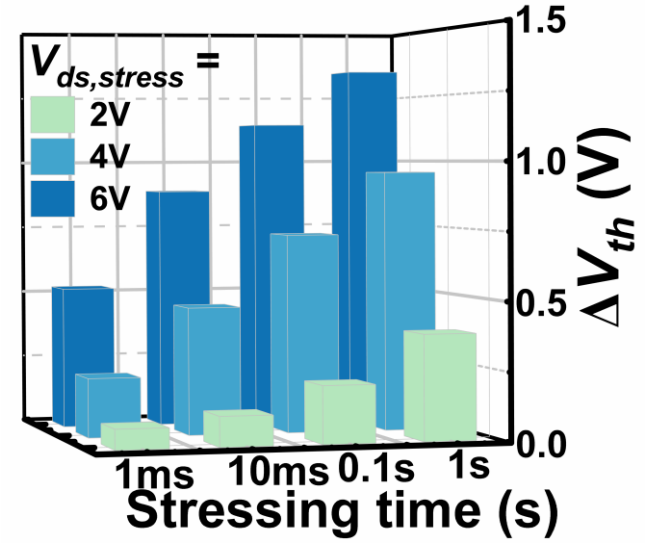

Fig. 8. The variation of ΔV_{th} with various $V_{ds,stress}$.

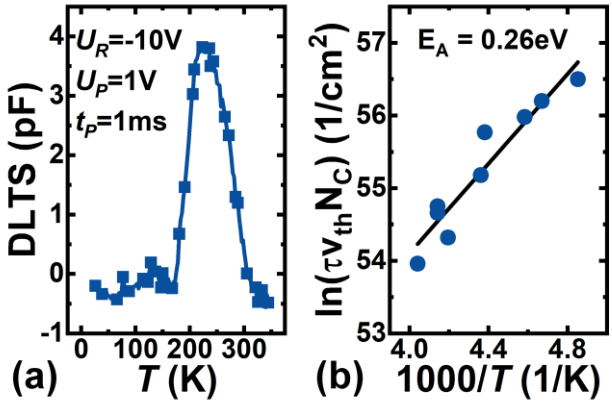

Fig. 9. (a) DLTS spectra from 25 K to 350 K. (b) Arrhenius plot of E1.

leading to the degradation of I_{ds} and shift of V_{th}. The findings reveal that bulk traps remain the primary contributor to device instability, emphasizing the critical importance of high-quality epitaxial growth for ensuring the stability of vertical devices.

V. Conclusion

In conclusion, a comprehensive investigation on dynamic instability of quasi-vertical GaN trench MOSFET with or without TBD is reported. When the devices operate in on-state, a larger V_{th} and a reduced I_{ds} are obtained with extending on-state duration. This I_{ds} degradation in the on-state is caused by gate and drain stressing voltage. The short-term time-resolved I_{ds} confirms the variation of I_{ds} in on-state for a switching cycle. The results demonstrate a current collapse of 21% in the device with TBD, outperforming 39% observed in MOSFETs without TBD. Furthermore, even after 500 repeated switching cycles under a $V_{gs,stress}$ of 6 V, the TBD device maintains a limited current collapse of only 10% for a short t_{on}. NBTI measurement displays the effect of $V_{gs,stress}$ on the V_{th}, a V_{th} shift of 1 V is recorded with a gate stressing of 6 V, which is attributed to electron capture at the dielectric/GaN interface. In addition, exposure to off-state drain bias stressing also induces a

decreased I_{ds}, amounting to 57.6% under a $V_{ds,stress}$ of 8V measured in DCTs. This reduction in current is accompanied by a positive shift in V_{th}. A ΔV_{th} of 1.34 V can be obtained with a $V_{ds,stress}$ of 6 V for the stressing time of 1 s. This deterioration in conduction characteristics is attributed to traps in the n^--GaN layer, with a capture activation energy of 0.26 eV extracted by DLTS. These findings collectively indicate that quasi-vertical GaN MOSFETs with TBD exhibit improved gate stability. Bulk traps remain the predominant factor contributing to device instability, underscoring the crucial significance of high-quality epitaxial growth for maintaining the stability of vertical devices. The detailed analysis of the impact of gate and drain stressing on conduction performance provides valuable insights for optimizing the overall performance of GaN quasi-vertical MOSFET devices.

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