Fabrication and Characterization of High-Voltage LEDs Using Photoresist-Filled-Trench Technique

Xinbo Zou, *Member, IEEE*, Yuefei Cai, Wing Cheung Chong, and Kei May Lau, *Fellow, IEEE*

***Abstract*—We report design, fabrication, and characterization of high-voltage LEDs (HVLEDs) using photoresist-filled-trench technique. Narrow trenches (1 μm wide) were etched to isolate the constituent LED cells of a HVLED chip and then passivated by refilling thermal curable photoresist. With a planarized HVLED surface, only a thin metal layer was needed for inter-cell connection. The narrow trench design ensured uniform light emission and allowed for negligible connection resistance. The optical power of a HVLED with 33 cells reached 1.76 W at 100 mA. The results suggested that HVLED is a viable design option for high-voltage and low current drive applications, with large and uniform light emission areas.**

***Index Terms*—High-voltage LEDs, indium bonding, large area LEDs, surface planarization, trench-filling technique.**

I. Introduction

GaN-BASED light-emitting diodes (LEDs) have been gaining considerable grounds in applications such as display, backlight units, automobile headlamps, and general illumination due to their high energy efficiency, long lifetime, and non-toxicity [1], [2]. In order to meet the increasing demand for large optical output power from GaN LEDs, the LED chip size and operation current are typically increased for conventional LEDs. However, issues such as current crowding and notorious "efficiency droop" may occur at high injection current for such single-junction large die LEDs. To alleviate these issues, techniques such as lattice-matched InAlGaN barrier [3], graded [4] or thick [5] quantum well (QW) thickness, or growth of QWs on semipolar/nonpolar planes [5], [6] have been reported, but these methods often involve complicated growth structure or expensive semipolar/nonpolar GaN substrates.

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X. Zou and K. M. Lau are with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong, and also with the Hong Kong University of Science and Technology (HKUST) Jockey Club Institute for Advanced Study, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong (e-mail: eexinbo@ust.hk; eekmlau@ust.hk).

Y. Cai and W. C. Chong are with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong (e-mail: ycaiag@connect.ust.hk; eeeddie@connect.ust.hk).

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An alternative method to mitigate the current crowding and therefore efficiency droop in conventional LED structures is to fabricate a single-chip high-voltage LED (HVLED) that consisted of multiple series-connected LED cells. An HVLED is typically operated at a low current injection in comparison with conventional low voltage/high current operation mode of single junction LEDs. As the constituent cell size of a HVLED is typically designed to be comparable with the current spreading length [7], in the range of several hundred micron, HVLED exhibits favorable current spreading and thereby achieves high output power efficiency. With operation voltages closer to mains or DC voltage supplies, HVLED also enables simplified LED driver design.

In connecting multiple LED cells in series, wire-bonding and/or monolithic metal interconnection are two common means for constructing HVLEDs. Connecting conventional LEDs in series by bond wires often suffers from reliability issues of the series connections and associated parasitic components. It is more favorable to fabricate monolithic HVLED chips using an *in-situ* metal-based interconnection on the chip [8]. To that end, proper cell isolation and sidewall passivation are two key process steps before deposition of a connecting metal layer. An inclined sidewall structure has been proposed by T. Zhan, *et al.* for better metal coverage in connecting adjacent LED cells [9]. However, complicated dry etch process was needed together with a relatively large gap area between LED cells. A dielectric layer such as SiO_2 [7], Al_2O_3 was widely adopted for sidewall passivation, but typically a thick metal layer (over 1 μm thick) [10], [11] and thereby long deposition time is needed to guarantee good metal coverage at the passivated sidewalls and connection between LED cells. It has also been reported that a thick Al metal connection layer may lead to Al whisker formation and cause failure in the HVLED burn-in test [12].

Polymer-based trench filling technique [13] which could be easily applied by spin-coating has been widely adopted in surface planarization and device passivation [14]–[17]. Li *et al.* [16] reported improved HVLED fabrication yield using a SU-8 passivation method. In this paper, we report fabrication and characterization of HVLED chips using photoresist-filled-trench and indium-bonding techniques. The fabricated HVLED features narrow inter-cell gaps ($\sim$1 μm wide for good wafer area utilization) and a thin metallization layer ($\sim$330 nm) for interconnection. Moreover, the flip-chip indium-bonding technique enabled integrating multiple HVLED chips to accommodate higher voltage ($>$100 V) and light output requirements. The fabricated HVLED chips demonstrated in this paper show good potential in applications which require

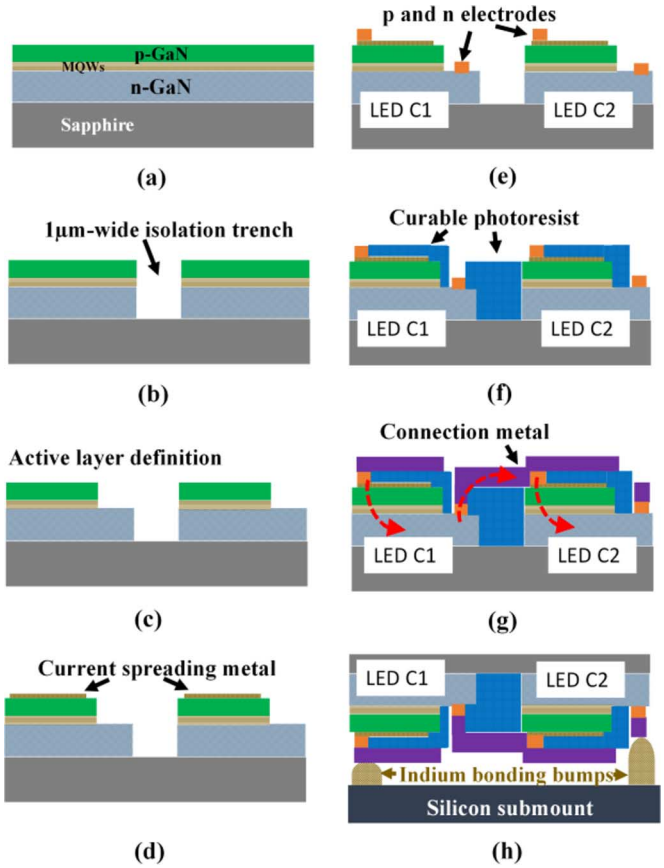

Fig. 1. Schematics of HVLED (two LED cells C1 and C2 drawn for illustration) fabrication process flow: (a) LED structure; (b) isolation trench etching; (c) active layer definition; (d) current spreading metal deposition; (e) p and n electrode metal deposition; (f) trench filling and sidewall passivation by curable photoresist; (g) connection metal deposition: current direction indicated by dotted-line arrows from LED C1 to C2; (h) wafer flip-chip bonding onto a Si submount by indium bonding.

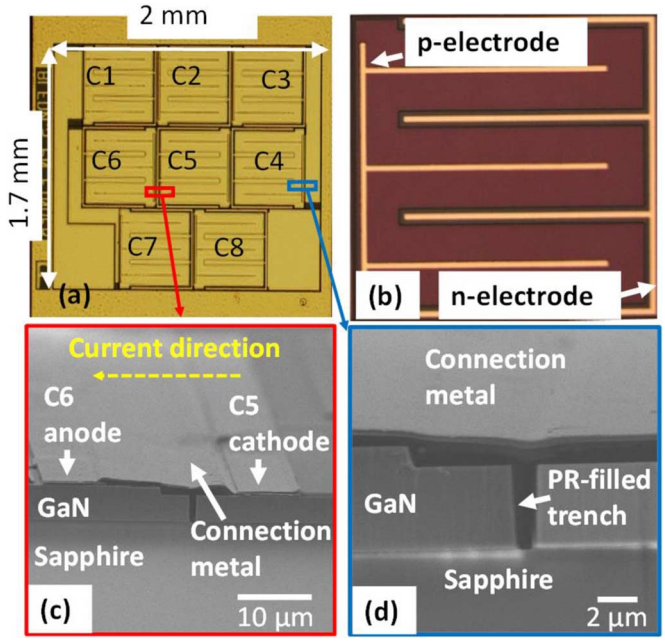

Fig. 2. (a) An optical microscopic image of a HVLED consisting of 8 LED cells. (b) Inter-digital electrode design used in a 500 μm $\times$ 500 μm LED cell. (c) tilted view SEM image showing metal interconnection between C5 cathode and C6 anode. (d) Cross-sectional SEM image showing isolation trench was refilled by thermal curable photoresist without voids.

uniform and large light output, and can be easily modified to accommodate any total voltage or power specifications for various applications.

II. Experiment

The GaN LEDs used in this study were grown on 2-inch planar or patterned sapphire substrates (pss). The epilayers included an un-doped GaN buffer layer, a Si-doped n-type GaN layer, InGaN/GaN multiple quantum wells (MQWs), and an Mg-doped p-type GaN layer [Fig. 1(a)]. 1 μm wide trenches between 500 μm $\times$ 500 μm LED cells were etched down to the sapphire substrate by ICP using SiO_2 as dry-etching masks [Fig. 1(b)]. After LED cell isolation, active regions of individual LED cells were further defined by inductively coupled plasma (ICP) dry etching [Fig. 1(c)]. Then a layer of 115 nm indium tin oxide (ITO) was deposited onto the mesas by E-beam evaporation and annealed to form a transparent current spreading layer (CSL) for individual LED cells [Fig. 1(d)]. Cr/Al/Ti/Au was then deposited as p and n electrodes [Fig. 1(e)]. Subsequently transparent and thermal curable photoresist[1] was spin-coated on the surface of LED cells acting as trench filling material for planarization and sidewall passivation [Fig. 1(f)]. Followed by contact hole opening on this photoresist using photolithography, a Cr/Al/Ti/Au metal stack was deposited to connect individual LED cells to form a whole HVLED chip as well as serving as a highly reflective layer [Fig. 1(g)]. Then the sapphire substrate was thinned down from 470 μm to 200 μm and polished to minimize light absorption from the sapphire substrate. Finally, the HVLED chip was flip-chip bonded onto a silicon submount using an indium bonding method [18] so that light could be extracted from the thinned sapphire substrate side [Fig. 1(h)].

[1][Online]. Available: http://www.everlightchemical-ecbu.com/product_detail.asp?seq=19

III. Results and Discussion

Fig. 2(a) shows an optical microscopic image of a fabricated HVLED consisting of eight series-connected LED cells. The HVLED chip size is 2 mm $\times$ 1.7 mm and each LED cell size is 500 μm $\times$ 500 μm. The 8 LED cells are connected in-series for the current to flow from C1 to C8 sequentially. For each constituent LED cell, interdigitated p and n electrodes were designed to facilitate uniform current spreading along the LED cell area as shown in Fig. 2(b). The LED cells were closely arranged with 1 μm wide trenches in between for higher light emission area utilization. The cross-sectional SEM images taken near the isolation trench area showed that as a passivation layer, the thermal curable photoresist completely filled the narrow trenches which had a large aspect ratio of around 4, as shown in Fig. 2(d). The photoresist trench-filling method could be applied at room temperature which essentially eliminates any damage induced in the high-temperature passivation methods, such as SiO_2 deposition by plasma enhanced chemical vapor deposition (PECVD). Moreover, the photoresist trench-filling method is capable of filling high aspect-ratio trenches without voids, which are typically observed in dielectric passivation

by PECVD. As shown in the Fig. 2(c), by careful tuning of the photoresist spin-coating rate, the LED surface could be planarized with the curable photoresist filling the trench. As a result of the surface planarization, only a very thin metal layer (∼330 nm) is needed to ensure interconnection between adjacent LED cells. The cured photoresist showed no adhesion nor deformation issues after all the process steps including lithography, metal deposition/lift off, and indium bonding at 180°C, which indicated good stability and high reliability of the trench refilling method.

A light emission image of a fabricated HVLED, in which light output is uniformly distributed over all eight LED cells, is shown in Fig. 3(a). The image was taken by a CCD camera at 1 mA current injection to avoid camera saturation. The uniform light emission over the entire HVLED chip area was attributed to moderate LED cell size (500 μm × 500 μm) and interdigitated electrode design. The typical current-voltage characteristic of the 8-cell HVLED chip in Fig. 3(b) showed that a good linearity was observed between forward voltages of HVLED and its LED cell. The forward voltage of the eight-cell HVLED at 20 mA is 23.5 V, which is consistent with 8 times of single LED cell voltage (2.97±0.03 V). The narrow trench design results in negligible interconnection resistance between LED cells and at the same time ensures uniform light emission all over the chip area without noticeable emission gap. The measured reverse leakage current of a fabricated HVLED chip was 9 nA at −50 V, showing good passivation effects from cured photoresist.

As the HVLED was flip-chip bonded onto a silicon carrier and the light was extracted from the sapphire side, a highly reflective metal is desirable. As shown in Fig. 3(c), for HVLED on planar sapphire substrate, as the first Cr glue layer thickness was reduced from 20 nm to 2 nm and the reflective Al layer was increased from 200 nm to 300 nm, the light output power was improved from 42 mW to 86 mW at 40 mA. The optical power enhancement well matched the reflectance measurement results that the reflectance was increased from around 40% to more than 85% at 470 nm (not shown here) when reducing the first Cr glue layer thickness from 20 nm to 2 nm. As the injection current increased from 0 to 100 mA, the light output power of a flip-chip bonded HVLED on planar sapphire substrate was linearly increased to 181 mW. Using LEDs grown on patterned sapphire substrate (pss) for fabrication, at 100 mA without any surface roughening or encapsulation the LOP could be boosted from 181 mW to 498 mW resulting from much enhanced light extraction efficiency [19] induced by photon scattering at the uneven GaN/pss interface. Considering the fact that the photoresist has high transmittance (>92% at 400 nm wavelength) the inter-connecting metal in this design also served as the reflective metal, which could greatly mitigate process complexity and save fabrication cost and time. Fig. 3(d) showed the wavelength shift as the injection current was increased from 0 to 60 A/cm^2 for a HVLED chip on a planar substrate. The peak wavelength was firstly blue-shifted (471 nm to 467 nm) due to a band-filling effect at relatively low current injection. As the injection current was further increased, the wavelength was only slightly red-shifted (467 nm to 472 nm) which was attributed to good heat dissipation of the Si submount and indium bonding layer. The small change in emission wavelength indicates low junction temperature of the flip-chip HVLED under high-power operation conditions.

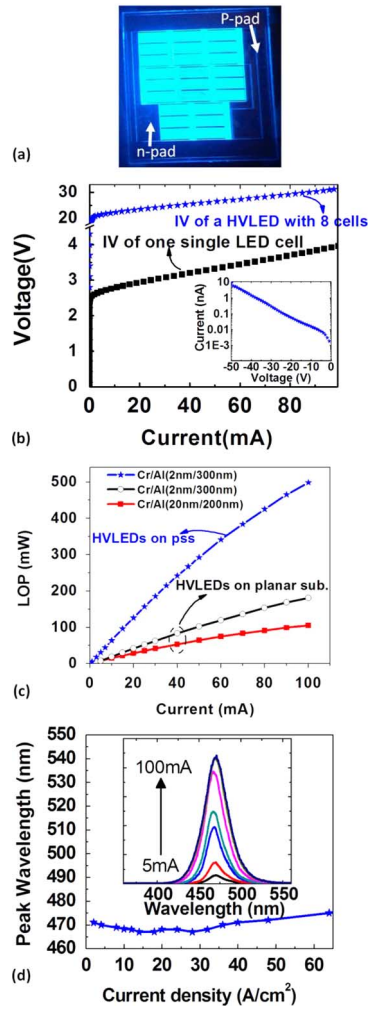

Fig. 3. (a) Light emission image of a HVLED chip; (b) I-V characteristics of a HVLED with eight series-connected LED cells in the forward voltage range; inset: in the reverse voltage range; (c) Light output power-current dependence of HVLEDs on pss and planar sapphire substrates; (d) HVLED peak wavelength-current relationship.

The photoresist-filled-trench technique could be applied to fabrication of HVLED with any number of LED cells without changing any passivation and connection parameters. As shown in Fig. 4(a), each HVLED chip consisted of eleven 500 μm × 500 μm LED cells and the trenches in between were kept as 1 μm wide and filled/passivated by the same photoresist technique. The planarized HVLED surface also facilitated the indium bonding process that an indium layer as thin as 1.5 μm was sufficient to bond the HVLED chip onto the Si submount. The indium flip-chip bonding technology also provides flexibility in bonding two or more HVLED chips onto one silicon submount to accommodate even higher forward voltage and larger output power demand. Fig. 4(a) illustrated that three HVLED chips were bonded onto one silicon substrate and connected in series by a pre-patterned metal layer on the Si platform. Adopting a highly reflective metal, the optical power of the whole chip measured from the sapphire side was 250 mW at 10 mA, which is translated to a wall plug efficiency

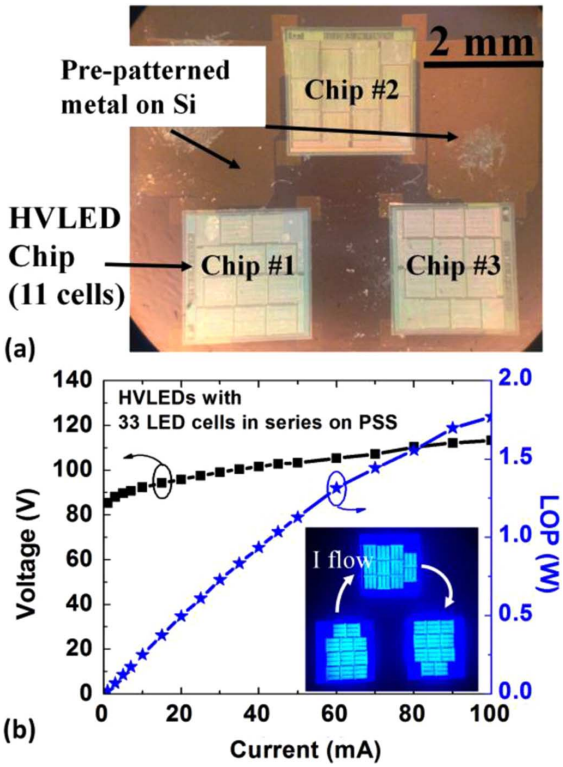

Fig. 4. (a) Optical microscopic image showing three HVLED chips were integrated by pre-patterned metal on a silicon submount. (b) *L–I–V* characteristics of the whole HVLED chip consisting of 33 cells on patterned sapphire substrates. Inset: light emission image of the whole HVLED chip with arrows indicating the current flow.

of 27.1%. The HVLEDs showed comparable power conversion efficiency to state-of-the-art HVLEDs without sapphire laser lift-off process reported in the literature [17], [20], with a larger emission area and smaller trench width. At 100 mA, the optical power of the whole HVLED chip reached 1.76 W and the forward voltage of the HVLED was 118 V, which is much closer to mains supply voltage in comparison with conventional high power LEDs allowing much simplified driver design. Moreover, the LED cell number could be flexibly adjusted to meet different working voltage requirement in a wide range. The large light output power from the HVLED chip made it suitable for applications which need large and uniform lighting area.

IV. Summary

In summary, we demonstrated a method for fabrication of HVLED chips using thermal curable photoresist as the trench filling and sidewall passivation material. After trench filling and surface planarization, only a thin metal layer (∼330 nm) is needed to connect constitute LED cells and at the same time severed as reflective metal. The narrow trench design ensured uniform light output power and allowed for negligible connection resistance. Good current spreading and thermal management have also been achieved using interdigitated electrode design and flip-chip bonding method. The light output power of HVLED with thirty-three cells reached 1.76 W at 100 mA after flip-chip bonding, without any surface roughening or silicone packaging. The planarized HVLED surface also guarantee high bonding yield and it is highly practical to bond two or more HVLED chips onto one silicon submount to accommodate even higher forward voltage and larger output power demand.

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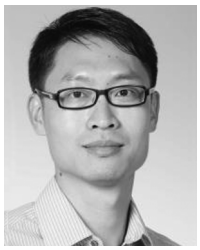

Xinbo Zou (M'14) received the B.E. degree in electronic engineering from Beijing University of Posts and Telecommunications (BUPT) in 2007, and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST) in 2013.

He is currently a Research Assistant Professor with the Department of Electronic and Computer Engineering, HKUST. His research interest includes growth, fabrication, and characterization of GaN-based device and nanostructures.

Yuefei Cai received the Bachelor and Master degrees from Harbin Institute of Technology, China, in 2011 and 2013, respectively, and is currently working toward the Ph.D. degree in the Department of Electronic and Computer Engineering, the Hong Kong University of Science and Technology, Hong Kong.

His current research interests include the design and fabrication of GaN-based devices.

Wing Cheung Chong received the Bachelor degree (highest honors) and M.Phil. degrees in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST), in 2005 and 2007, respectively, where he is currently working toward the Ph.D. degree at the Electronic and Computer Engineering Department.

In his postgraduate study, he is involved in the research of cost-effective, high brightness LED processing techniques, and next generation LED-based micro-display technology.

Kei May Lau (S'78–M'80–SM'92–F'01) received the B.S. and M.S. degrees in physics from the University of Minnesota, Minneapolis, MN, USA, and the Ph.D. degree in electrical engineering from Rice University, Houston, TX, USA.

She was on the ECE faculty at the University of Massachusetts—Amherst. She is currently a Chair Professor at the Hong Kong University of Science and Technology (HKUST), engaging in compound semiconductor materials and device research for high-speed and photonic applications.