High Performance Monolithically Integrated GaN Driving VMOSFET on LED

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***Abstract*— This letter reports the monolithic integration of GaN-based driving vertical metal–oxide–semiconductor field-effect transistor (VMOSFET) on light-emitting diode (LED) with high output current density and brightness. By selectively regrowing a simple p- and n-GaN bilayer on top of an LED wafer, the VMOSFET was realized with an n/p/n structure and intrinsically connected with the LED through the bottom conductive n-GaN layer. During the fabrication, a tetramethylammonium hydride wet etch technique was employed to smoothen the sidewall channel surface of the VMOSFET and to enhance its channel electron mobility, consequently achieving a high output current density exceeding 1.4 kA/cm^2. The integrated VMOSFET-LED exhibited a high light output power of 8.5 mW or 9.4 W/cm^2 with a modulated injection current of 10 mA through the VMOSFET, showing a great potential of such integration scheme for a variety of smart-lighting applications.**

***Index Terms*— Enhancement-mode, GaN, light-emitting diode, monolithic integration, vertical metal-oxide-semiconductor field effect transistor.**

I. Introduction

LIGHT emitting diode (LED) technologies for lighting and displays generally require dedicated electronic driving circuits, such as AC-DC power conversion, current source, and dimming control using pulse-width modulation (PWM) methods [1], [2]. The traditional LED drivers are typically implemented with discrete components and bulky in size. The parasitic elements due to bonding-wires may lead to a high power consumption and low efficiency of the drivers. Moreover, the failure of an LED system is usually caused by its peripheral components and packaging rather than the LED device itself. Integration of LEDs with on-chip driving electronics is promising in circumventing these issues and has received remarkable research interest in recent years [3].

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III-nitride materials provide a common platform for integrating light emitters and their driving electronics, such as GaN blue LEDs and field effect transistors (FETs) [4], [5]. Compared with conventional silicon devices, GaN FETs are essentially good candidates for LED drivers due to their superior properties such as large breakdown voltage, high operation speed, low power loss, and high temperature endurance [6]–[9]. By integrating GaN-based LEDs and driving transistors on the same substrate, a compact smart-lighting system can be realized and benefit a range of applications such as solid-state lighting, micro-displays and visible light communications (VLCs) [10]–[13].

Previously, monolithic integration of GaN-based LEDs with lateral-type depletion-mode (D-mode) transistors, such as AlGaN/GaN high electron mobility transistor (HEMT) [10]–[12] and metal-oxide-semiconductor field effect transistor (MOSFET) [13], has been demonstrated using either selective epitaxial growth (SEG) or selective epitaxial removal (SER) methods. We recently proposed an alternative integration approach: integrate enhancement-mode (E-mode) vertical MOSFET on a standard LED structure [14]. Firstly, E-mode devices can improve the reliability of the LED system by simplifying the driving circuits with a single-polarity voltage supply. Secondly, VMOSFETs share similar junction-based vertical structures with LEDs and are more suitable for integration than the lateral ones [14]–[16]. However, the unoptimized GaN crystalline quality and unwanted dry etching damage existed at the channel sidewall masked the advantages of the proposed integration scheme.

In this letter, we demonstrate the monolithic integration of LED with driving VMOSFET using a high-quality GaN LED epi-wafer grown on a patterned sapphire substrate (pss) and developing a tetramethylammonium hydride (TMAH) wet etch technique to remove damage from the etched sidewall channel surface of the VMOSFET. The integrated VMOSFET-LED device exhibited greatly improved brightness and output current density.

II. Experiment

The GaN LED epi-wafer used in this study were grown on a 2-inch pss. The epilayers consisted of an un-doped GaN buffer layer, a Si-doped n-type GaN layer, InGaN/GaN multiple quantum wells (MQWs), and an Mg-doped p-type GaN layer. Fig. 1 schematically shows the main steps in fabricating the monolithically integrated VMOSFET-LED device. To start with, a 200 nm SiO_2 was deposited on the LED wafer by plasma enhanced chemical vapor deposition (PECVD) and then patterned using a buffered oxide etchant (BOE), serving as the regrowth mask. Afterwards, a p- and n-GaN bilayer

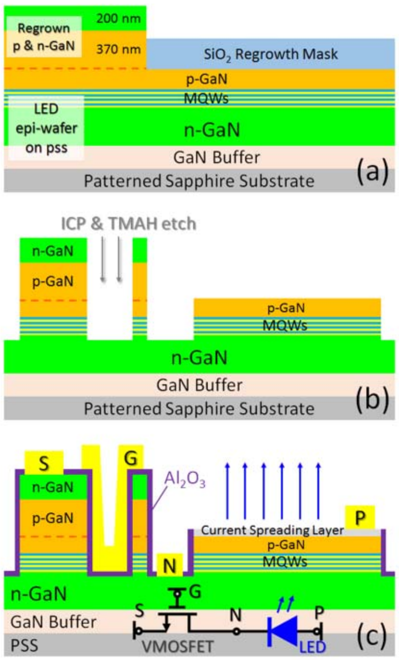
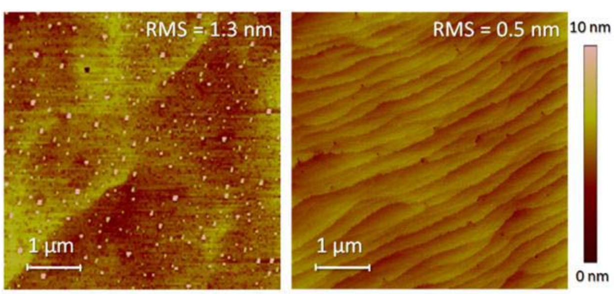


Fig. 1. Schematics of the main steps in fabricating monolithically integrated VMOSFET-LED device: (a) selectively regrow a p- and n-GaN bilayer on LED; (b) gate trenches and device isolation etching; (c) fully processed device.



(a) (b)

Fig. 2. AFM images of the LED epi-wafer before (a) and after (b) GaN bilayer regrowth.

was selectively grown on the exposed region to form an n/p/n structure for the VMOSFETs [Fig. 1(a)]. Trimethylgallium (TMGa) and ammonia (NH_3) were used as precursors for Ga and N, respectively. The p-GaN layer was 370 nm thick with an Mg dopant concentration of around 3×10^{19} cm^{-3}, while the 200 nm n-GaN layer had a two-step doping profile (Si doping level: $\sim1\times10^{19}$ cm^{-3} for the first 180 nm and up to 5×10^{19} cm^{-3} for the remaining 20 nm). Fig. 2 compares the atomic force microscopy (AFM) images of the LED epi-wafer (a) before and (b) after regrowth with a scanned area of 5×5 μm^2. Small dots with a very high density appeared on the as-grown LED surface, which could help to enhance the LED's light extraction efficiency. Attributed to the alleviated growth temperature of the upmost n-GaN layer, the root mean square (RMS) roughness was reduced from 1.3 nm to 0.5 nm after regrowth and well-aligned step flow patterns were observed.

After completely removing the SiO_2 regrowth mask by BOE, the gate trenches of the VMOSFETs and device isolation for both the LEDs and VMOSFETs were etched simultaneously using a Cl_2-based inductively coupled plasma (ICP) etch [Fig. 1(b)]. Following that, the sample was immersed into a 25% TMAH solution at 75 °C for 60 minutes. The TMAH wet etch was found effective in removing damage from the dry-etched GaN sidewall [17]. To activate the regrown p-GaN layer, a rapid thermal annealing (RTA) was performed at 800 °C for 1 minute in a N_2 ambient. The nominal hole concentration was around 2×10^{17} cm^{-3}. A 30 nm Al_2O_3 gate dielectric for the VMOSFETs was then blanket deposited on the sample surface by atomic layer deposition (ALD), while the Al_2O_3 in the LED region was removed by BOE. Subsequently, a Ni/Au current spreading layer for LEDs was deposited by e-beam evaporation followed by a RTA in an atmospheric ambient at 570 °C for 5 minutes. After opening the contact holes by BOE, a multi-layer metal stack Cr/Al/Ti/Au was evaporated to form both the n-electrodes for the LEDs and the source Ohmic contacts for the VMOSFETs. Finally, the Ni/Au gate metal of the VMOSFETs was deposited. Fig. 1 (c) depicts the cross-sectional schematic of a complete integrated VMOSFET-LED device. The LED and VMOSFET were serially connected through the highly conductive n-GaN layer, with no need of extra metal interconnections. As discussed previously [14], [18], the elimination of metal interconnection helped to reduce related parasitic components. The n-electrode between the integrated LED and VMOSFET was reserved for separately characterizing the two devices, as illustrated by the equivalent circuit diagram in the inset of Fig. 1(c).

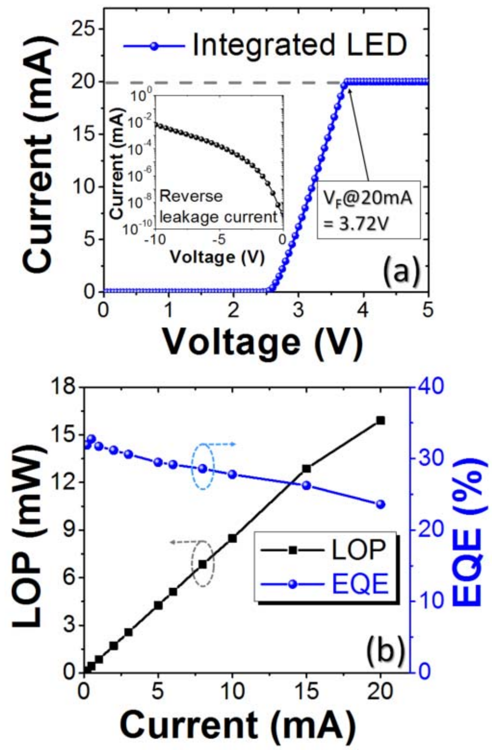


Fig. 3. (a) I-V and (b) LOP characteristics of the integrated LED. The inset shows the LED's reverse leakage current.

III. Results and Discussion

Fig. 3(a) shows the I-V curve of the integrated LED measured between p and n electrodes. The forward voltage (V_F)

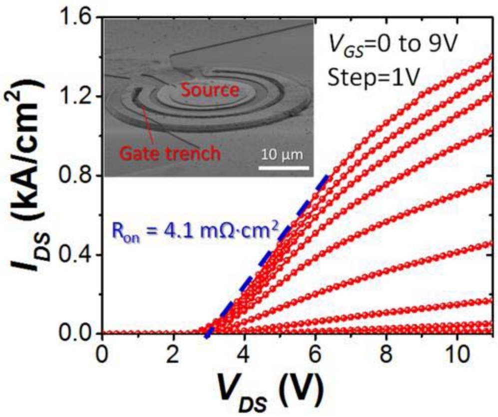


Fig. 4. Output characteristics of the integrated VMOSFET-LED device. The inset shows the SEM image of the circular-shaped VMOSFET.

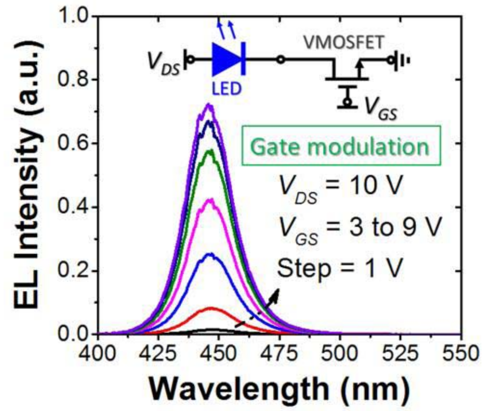


Fig. 5. EL spectra of the VMOSFET-LED modulated by gate biasing at $V_{DS} = 10$ V. The inset shows the circuit configuration of the integrated device.

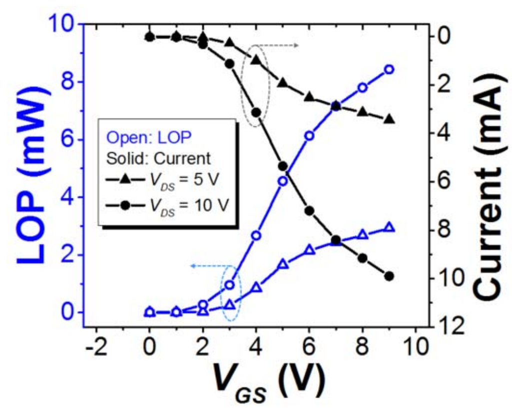


Fig. 6. Gate modulated LOP and I–V characteristics of the integrated VMOSFET-LED device at different drain biases.

of the 300 μm × 300 μm LED was 3.72 V at an injection current of 20 mA. As shown in the inset of Fig. 3(a), the leakage current of the LED was below 10^{-2} mA at a reverse bias of -10 V. Fig. 3(b) plots the light output power (LOP) and external quantum efficiency (EQE) versus the injection current of the LED. The device exhibited a relatively high LOP of 16 mW at an injection current of 20 mA, corresponding to an EQE of 23.5%. The peak EQE of ~33% was observed at a relatively small injection current density of ~600 mA/cm^2. The dramatic improvement in LED brightness compared to the previously reported integration schemes was mainly attributed to the better crystalline quality of LED epi-wafer grown on pss than those grown on planar sapphire substrates.

The output characteristic of the integrated VMOSFET-LED device is plotted in Fig. 4. It can be seen that the injected current through the VMOSFET-LED device can be well controlled by the gate and drain supply voltages (V_{GS} and V_{DS}) of the VMOSFET. The inset shows the scanning electron microscopy (SEM) image of the circular-shaped VMOSFET, who has a diameter of 30 μm. The VMOSFET was E-mode with a threshold voltage of +1.8 V. The I-V curve of the integrated device showed a turn-on voltage of around 3 V, which resulted from the serially connected LED. The maximum output current density was measured to be 1.4 kA/cm^2 at $V_{DS} = 11$ V and $V_{GS} = 9$ V, leading to a low specific on-resistance (R_{on}) of 4.1 mΩ·cm^2. Compared to the device without TMAH treatment [14], the output current density in this study was increased by over one order of magnitude, demonstrating that the TMAH wet etch technique was very effective in smoothing the sidewall channel surface of the VMOSFET and enhancing its channel electron mobility. Further improvement of the output current density can be achieved by optimizing the VMOSFET layout, such as using polygonal cells to increase the channel density [15].

Fig. 5 shows the electroluminescence (EL) spectra of the integrated VMOSFET-LED with a fixed V_{DS} of 10 V but various V_{GS}. The device emitted blue light ($\lambda \approx 440$ nm) with the intensity modulated by gate biasing. Fig. 6 presents the modulation in emission brightness of the integrated VMOSFET-LED by both V_{GS} and V_{DS} though the injection current from the driving transistor. In such integration, current-controlled LED has been converted to voltage control mode, which is much simpler to work with. No light emission could be observed when the E-mode VMOSFET was pinched off at $V_{GS} < 1.8$ V. While $V_{GS} = 9$ V and $V_{DS} = 10$ V, the integrated device exhibited a high LOP of 8.5 mW or 9.4 W/cm^2 with a low injection current of 10 mA through the VMOSFET. To our knowledge, this is the best performance ever reported for monolithic integration of GaN LEDs with driving transistors [19]. Nevertheless, the high V_{DS} of the integrated VMOSFET-LED lead to a high power consumption. The drive voltage can be reduced by increasing the VMOSFET's device size to improve its drive capability.

IV. Conclusion

In conclusion, a monolithically integrated VMOSFET-LED device with enhanced output current density and brightness has been developed using a GaN LED epi-wafer grown on pss. The TMAH wet etch technique was proven highly effective in improving the channel electron mobility of the VMOSFET. The superior device performance in this study successfully demonstrated the viability of the proposed integration scheme.

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References

[1] H.-J. Chiu, Y.-K. Lo, J.-T. Chen, S.-J. Cheng, C.-Y. Lin, and S.-C. Mou, "A high-efficiency dimmable LED driver for low-power lighting applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 735–743, Feb. 2010, doi: 10.1109/TIE.2009.2027251.

[2] J. J. D. McKendry, D. Massoubre, S. Zhang, B. R. Rae, R. P. Green, E. Gu, A. E. Kelly, and M. D. Dawson, "Visible-light communications using a CMOS-controlled micro-light- emitting-diode array," *J. Lightw. Technol.*, vol. 30, no. 1, pp. 61–67, Jan. 1, 2012, doi: 10.1109/JLT.2011.2175090.

[3] K. M. Lau, H. W. Choi, S.-W. R. Lee, P. K. T. Mok, J. K. O. Sin, C. P. Yue, and W.-H. Ki, "Cost-effective and eco-friendly LED system-on-a-chip (SoC)," in *Proc. 10th China Int. Forum Solid State Lighting (ChinaSSL)*, Beijing, China, 2013, pp. 235–238.

[4] M. H. Crawford, "LEDs for solid-state lighting: Performance challenges and recent advances," *IEEE J. Sel. Topics Quantum Electron.*, vol. 15, no. 4, pp. 1028–1040, Jul./Aug. 2009, doi: 10.1109/JSTQE.2009.2013476.

[5] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008, doi: 10.1109/JPROC.2007.911060.

[6] S. Bandyopadhyay, B. Neidorff, D. Freeman, and A. P. Chandrakasan, "90.6% efficient 11MHz 22W LED driver using GaN FETs and burst-mode controller with 0.96 power factor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2013, pp. 368–369, doi: 10.1109/ISSCC.2013.6487773.

[7] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. D. Margomenos, and M. Micovic, "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 2982–2996, Oct. 2013, doi: 10.1109/TED.2013.2268160.

[8] M. Kuzuhara and M. Tokuda, "Low-loss and high-voltage III-nitride transistors for power switching applications," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 405–413, Feb. 2015, doi: 10.1109/TED.2014.2359055.

[9] X. Lu, J. Ma, H. Jiang, C. Liu, P. Xu, and K. M. Lau, "Fabrication and characterization of gate-last self-aligned AlN/GaN MISHEMTs with *in situ* SiN_x gate dielectric," *IEEE Trans. Electron Devices*, vol. 62, pp. 1862–1869, Jun. 2015, doi: 10.1109/TED.2015.2421031.

[10] Z. Li, J. Waldron, T. Detchprohm, C. Wetzel, R. F. Karlicek, Jr., and T. P. Chow, "Monolithic integration of light-emitting diodes and power metal-oxide-semiconductor channel high-electron-mobility transistors for light-emitting power integrated circuits in GaN on sapphire substrate," *Appl. Phys. Lett.*, vol. 102, no. 19, pp. 192107-1–192107-3, May 2013, doi: 10.1063/1.4807125.

[11] Z. J. Liu, T. Huang, J. Ma, C. Liu, and K. M. Lau, "Monolithic integration of AlGaN/GaN HEMT on LED by MOCVD," *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 330–332, Mar. 2014, doi: 10.1109/LED.2014.2300897.

[12] F. G. Kalaitzakis, E. Iliopoulos, G. Konstantinidis, and N. T. Pelekanos, "Monolithic integration of nitride-based transistor with light emitting diode for sensing applications," *Microelectron. Eng.*, vol. 90, pp. 33–36, Feb. 2012, doi: 10.1016/j.mee.2011.04.067.

[13] Y.-J. Lee, Z.-P. Yang, P.-G. Chen, Y.-A. Hsieh, Y.-C. Yao, M.-H. Liao, M.-H. Lee, M.-T. Wang, and J.-M. Hwang, "Monolithic integration of GaN-based light-emitting diodes and metal-oxide-semiconductor field-effect transistors," *Opt. Exp.*, vol. 22, no. S6, pp. A1589–A1595, 2014, doi: 10.1364/OE.22.0A1589.

[14] X. Lu, C. Liu, H. Jiang, X. Zou, A. Zhang, and K. M. Lau, "Monolithic integration of enhancement-mode vertical driving transistorson a standard InGaN/GaN light emitting diode structure," *Appl. Phys. Lett.*, vol. 109, no. 5, p. 053504, 2016, doi: 10.1063/1.4960105.

[15] O. Tohru, I. Tsutomu, U. Yukihisa, and N. Junya, "1.8 $m\Omega \cdot cm^2$ vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation," *Appl. Phys. Exp.*, vol. 8, no. 5, p. 054101, 2015, doi: 10.7567/APEX.8.054101.

[16] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistors on GaN Bulk Substrates," *Appl. Phys. Exp.*, vol. 1, p. 011105, 2008, doi: 10.1143/APEX.1.011105.

[17] M. Kodama, M. Sugimoto, E. Hayashi, N. Soejima, O. Ishiguro, M. Kanechika, K. Itoh, H. Ueda, T. Uesugi, and T. Kachi, "GaN-based trench gate metal oxide semiconductor field-effect transistor fabricated with novel wet etching," *Appl. Phys. Exp.*, vol. 1, no. 2, p. 021104, 2008, doi: 10.1143/APEX.1.021104.

[18] C. Liu, Y. Cai, Z. Liu, J. Ma, and K. M. Lau, "Metal-interconnection-free integration of InGaN/GaN light emitting diodes with AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 106, no. 18, pp. 181110-1–181110-4, May 2015, doi: 10.1063/1.4921049.

[19] C. Liu, Y. Cai, X. Zou, and K. M. Lau, "Low-leakage high-breakdown laterally integrated HEMT-LED via n-GaN electrode," *IEEE Photon. Technol. Lett.*, vol. 28, no. 10, pp. 1130–1133, May 2016, doi: 10.1109/LPT.2016.2532338.