Journal of Crystal Growth 370 (2013) 265–268

Contents lists available at SciVerse ScienceDirect

Journal of Crystal Growth

journal homepage: www.elsevier.com/locate/jcrysgro

Improved GaN-based LED grown on silicon (111) substrates using stress/dislocation-engineered interlayers

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ARTICLE INFO

Available online 16 November 2012

Keywords:
A1 Crystal structure
A1. Defects
A1. Stresses
A3. Metalorganic vapor phase epitaxy
B1. Nitrides
B3. Light emitting diodes

ABSTRACT

We report the growth of high crystalline quality GaN-based light emitting diodes (LEDs) on Si (111) substrates with AlN/GaN superlattice interlayer for both stress and dislocation engineering. A focused study involved comparison of different interlayer structures including low-temperature AlN, medium-temperature AlN multilayers and AlN/GaN supperlattice for optimization of the LED performance. The results show that the AlN/GaN supperlattice interlayer is the most effective in reducing the residual tensile stress and improving the crystalline quality of GaN on Si. With the AlN/GaN superlattice interlayer, optical properties of the LEDs were enhanced and optical output power of unpackaged LED chips on Si substrates was improved by 24%.

1. Introduction

Si substrate for fabrication of GaN-based LEDs has attracted great attention recently, primarily because of its availability in large wafer size and potentially lower manufacturing cost of solid state lighting when compared with sapphire or SiC substrates [1]. In addition, the growth of GaN-based LEDs on Si allows good thermal management as Si has a better thermal conductivity than sapphire. Nowadays, most high performance LEDs requires removal of the substrate for better heat dissipation and optical output. Si can be removed by conventional wet etching [2] while sapphire requires expensive and elaborate laser liftoff.

The main difficulties in growing high-performance GaN-based LEDs on Si substrates are the large mismatch in lattice constant (16.9%) and thermal expansion coefficients (57%) between GaN and Si [3]. The huge mismatch in thermal expansion coefficients can cause thermal tensile stress and result in severe cracking of the GaN film during the post-growth cooling process. Additionally, the mismatch in lattice constant would generate large amount of dislocations in the order of 10^9–10^{10} cm^{-2} [1]. Many mitigating methods have been proposed to overcome these challenges. One commonly used means is to utilize a low-temperature AlN (LT-AlN) single interlayer for GaN on Si [4,5]. The LT-AlN interlayer can effectively reduce the crack density by compensating for the thermal tensile stress. However, it introduces new dislocations at the upper LT-AlN/GaN interface [6,7]. Also it is well known that there is a trade-off between the crystalline quality and the stress management for the LEDs on Si, when determining the growth temperature and thickness of the LT-AlN interlayer [8]. Lowering the temperature and increasing the AlN thickness can enhance the stress state, but more dislocations will be generated; increasing the temperature and decreasing the thickness can reduce the dislocation density, but there would be a higher risk of crack development. This trade-off relationship may put a limitation on further development of the GaN-based LEDs on Si. So there is great motivation to explore alternate interlayer structures which can not only improve stress and but also minimize dislocation formation/propagation for high-performance GaN-based LEDs grown on Si.

In this work, GaN-based LEDs on Si (111) substrates with different interlayer structures underneath were investigated. LT- AlN, medium-temperature AlN multilayer (MT-AlN ML) and AlN/GaN supperlattice (SL) were compared for the interlayer effect. Their influence upon the stress state and crystalline quality of the GaN is presented and analyzed. GaN-based LED structures were grown, fabricated and characterized. The results of unpackaged LED chips indicate that the stress management, crystalline quality and optical properties of the GaN-based LEDs on Si can be greatly enhanced by the AlN/GaN superlattice interlayer.

2. Experimental procedure

Six samples were grown on 2-in. Si (111) substrates using an AIXTRON2000HT MOCVD system. Trimethylgallium (TMGa), trimaluminum (TMAl), trimethylindim (TMIn) and ammonia (NH_3) were used as precursors for Ga, Al, In and N, respectively. Biscyclopen-tadienyl magnesium (Cp_2Mg) and silane (SiH_4) were

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http://dx.doi.org/10.1016/j.jcrysgro.2012.10.028

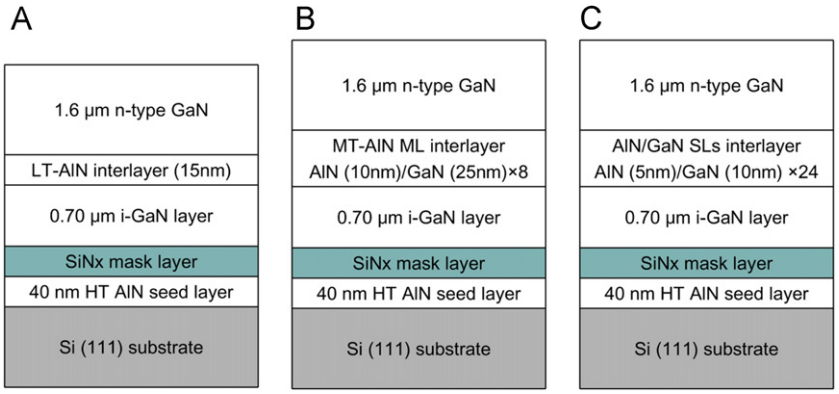

Fig. 1. Schematic of n-GaN samples on Si with different interlayer structures.

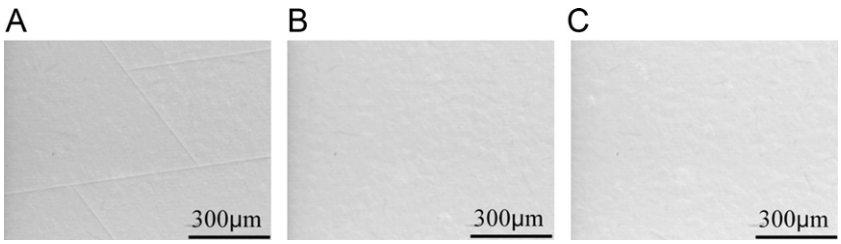

Fig. 2. Surface morphology of sample A, B and C under Nomarski interference optical microscopy.

used as the p- and n-type doping sources. H_2 and N_2 were used as carrier gases. To remove the native oxide on Si surfaces, the substrates were heated up to 1140 °C for 10 min under a H_2 ambience before growth. As shown in Fig. 1, three n-GaN samples (sample A, B and C) with 1.6 μm n-type GaN on top were first grown for material characterization. The net carrier concentration of the n-GaN layer was around $6\times10^{18}\,cm^{-3}$ from room-temperature Hall measurement and was kept constant throughout the experiment. These samples included an identical nucleation layer, a buffer layer and n-type GaN layer but different interlayers. The optimized growth temperatures for AlN of the LT-AlN (sample A), MT-AlN ML (sample B) and AlN/GaN SL (sample C) were 830 °C, 1020 °C and 1070 °C, respectively. After the growth, surface morphology of the samples was investigated with Nomarski interference optical microscopy and atomic force microscopy (AFM) from both macroscopic and microscopic scales. Raman scattering spectroscopy was used to evaluate the stress state of the samples. Crystalline quality of the n-GaN layers was studied by transmission electron microscopy (TEM) and the full width at half-maximum (FHWM) of both symmetric and asymmetric ω-rocking curves measured by high-resolution X-ray diffraction (XRD).

Furthermore, another three LED samples (LED-A, LED-B and LED-C) were grown for optical property characterization and device fabrication. The LED samples had an identical LED structure including a 1.6 μm n-GaN, five periods InGaN/GaN MQWs, 20 nm p-AlGaN layer and 150 nm p-GaN layers. LED-A, LED-B and LED-C had the same buffer and interlayer structures as sample A, B and C, respectively. Optical properties of the LED samples were studied by room-temperature Photoluminescence (PL). After that, LED chips on Si substrates were fabricated using a standard three-mask process and the optical output power of the unpackaged chips was measured.

3. Results and discussion

Optical micrographs of samples A, B and C are shown in Fig. 2. All the samples show smooth and shiny surfaces. However, cracks were observed for sample A. This indicates that the thermal tensile stress is not completely offset by the LT-AlN interlayer grown at 830 °C. However, both the MT-AlN ML interlayer and the SL interlayer can improve the stress state and 1.6 μm crack-free n-GaN was achieved, as shown in Fig. 2(b) and (c).

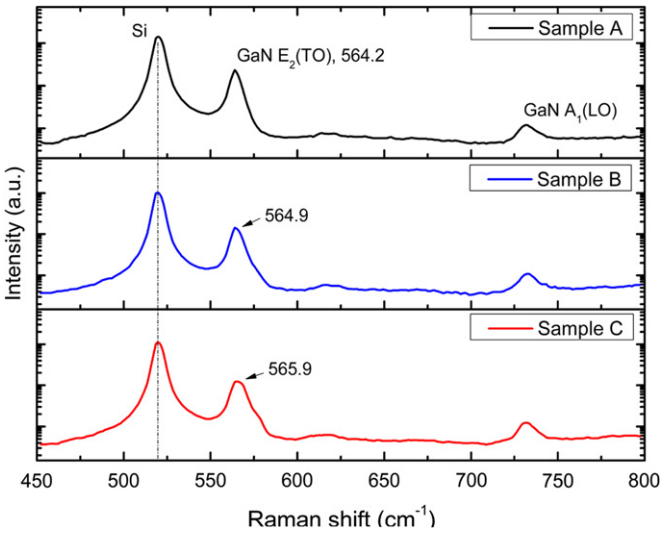

Fig. 3. Semilogarithmic Raman spectra of sample A, B and C.

Table 1
FWHM of symmetric (002) and asymmetric (102) ω-rocking curves for sample A, B and C.

Sample	(002) FWHM (arcsec.)	(102) FWHM (arcsec.)
Underlying i-GaN layer	611	854
A	601	1231
B	418	918
C	396	788

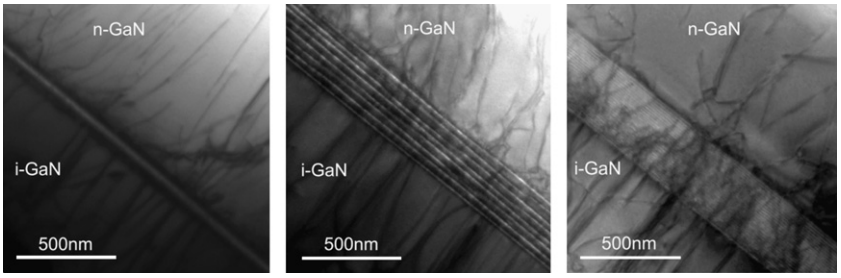

Fig. 4. Cross-sectional TEM images of sample A, B and C.

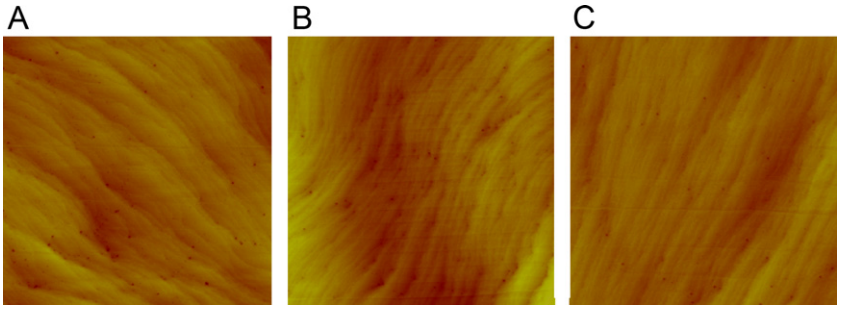

Fig. 5. AFM images of sample A, B and C. The scan area is 2 μm × 2 μm and the vertical scale is 10 nm for all samples.

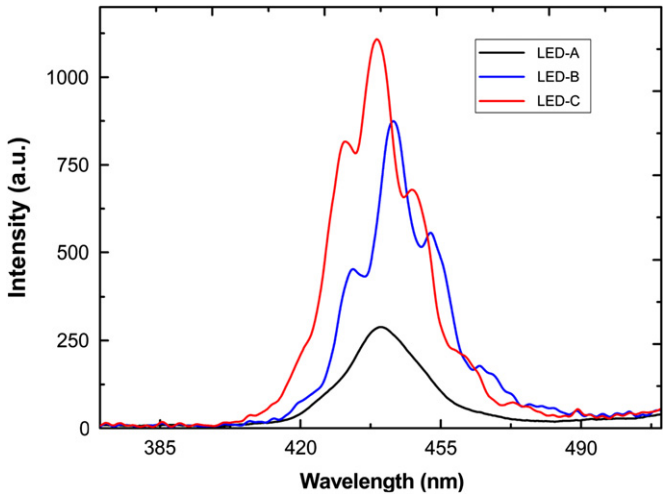

Fig. 6. PL spectrums of LED-A, LED-B and LED-C at room temperature with 325 nm He–Cd laser as the excitation source.

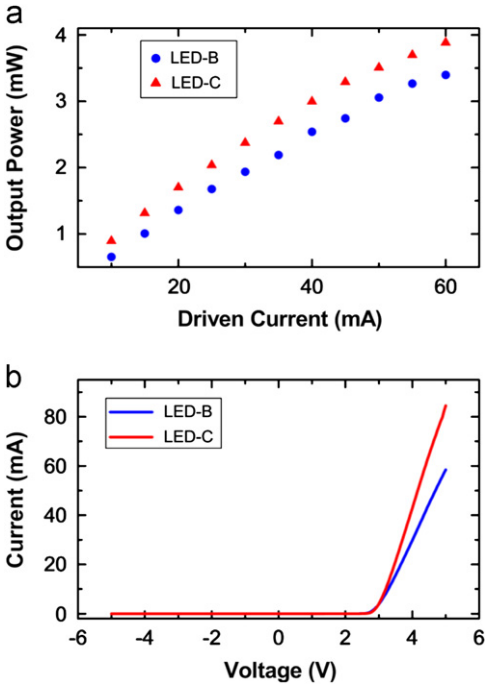

Fig. 7. (a) L–I and (b) I–V characteristics of LED-B and LED-C.

To further investigate the stress state of the samples, Raman scattering was carried out and the Raman spectra in a back-scattered geometry were shown in Fig. 3. Both GaN E_2 (high) (E_2^h), and A_1 (LO) phonon modes can be clearly observed. It is well known that the GaN E_2^h phonon peak is related to the residual stress inside the layer. With respect to the stress-free GaN E_2^h peak at 567.5 cm^{-1}, the residual tensile stress in the GaN layer can be estimated by

$$\Delta\omega = 4.3\sigma_{xx}\ cm^{-1}\ GPa^{-1} \quad (1)$$

where $\Delta\omega$ is the strain-induced shift of the E_2^h peak and σ_{xx} is the in-plane biaxial stress [9]. The GaN E_2^h peak positions of sample A, B and C were at 564.2 cm^{-1}, 564.9 cm^{-1} and 565.9 cm^{-1}, respectively. After calculation, it can be found that sample A suffers from the largest residual tensile stress, estimated to be 0.767 GPa. The tensile stress for sample B and C is estimated to be 0.604 GPa and 0.372 GPa, respectively. The results indicate that the AlN/GaN SL interlayer is much more effective in stress engineering for GaN on Si, when compared with the MT-AlN ML and LT-AlN interlayers. This can be explained by the fact that more AlN exist in the SL interlayer for strain balancing than the MT-AlN ML interlayer or LT-AlN interlayer, compensating more tensile strain for the upper n-GaN during the cooling process [8].

Crystalline quality of all three samples A, B and C were examined by XRD and the FWHM data for both symmetric (002) and asymmetric (102) ω-scan were listed in Table 1. Also the XRD results of an 700 nm underlying i-GaN layer (grown separately with the identical growth conditions) were provided in Table 1 for comparison. It is known that the (002) FWHM is related to the dislocations with screw component while the (102)

FWHM is related to the amount of edge dislocations. By comparing the FWHM data of sample A and B, it can be seen that the dislocation density of sample B is much smaller than that of sample A. This phenomenon can be attributed to two factors. Firstly, the higher growth temperature for the MT-AlN ML interlayer helps reduce the relaxation of the AlN layer on the lower GaN layer. Thus fewer dislocations were produced [8]. Secondly, with increasing number of AlN layers, some dislocations could be blocked while the dislocation generation at the upper AlN/GaN interface can be suppressed, due to the layer-by-layer enhancement of crystalline quality of the GaN layer below the AlN layer [10]. It was also noted that both sample A and B exhibited larger FWHM value than that of the underlying i-GaN layer. This indicates that the LT-AlN interlayer and the MT-AlN interlayer enlarge the dislocations density due to the lattice mismatch between AlN and GaN. Sample C has achieved the best FWHM of the n-GaN samples and its FWHM was well below that of the underlying i-GaN layer alone. This can be explained by the dislocation-filtering effect of the superlattice structure, in addition to the increased growth temperature and total AlN material in the AlN/GaN SL [11]. Fig. 4 shows the cross-sectional bright-field TEM images of the samples, collected near the GaN [1–100] zone axis. It can be observed that some of the dislocations bend and merge inside the SL interlayer, resulting in reduced dislocation density when compared with the LT-AlN or MT-AlN ML interlayers. This phenomenon is due to the elastic strain inside the SL, which can lead to the bending and annihilation of dislocations [12,13]. Therefore it can be concluded that the AlN/GaN SL interlayer is more effective in crystalline quality engineering for GaN on Si than the MT-AlN ML interlayer or the LT-AlN interlayer.

Surface morphology of the samples was investigated using atomic force microscopy (AFM) from the microscopic scale, as shown in Fig. 5. All of the three samples exhibit very smooth surfaces and clear atomic step flow patterns. The root-mean-square (RMS) roughness for sample A, B and C are 0.523 nm, 0.937 nm and 0.455 nm, respectively. Sample C having the smallest RMS and showing the best aligned atomic steps, indicates the best surface morphology among the three samples.

Room-temperature photoluminescence (PL) for the three LED samples (LED-A, LED-B and LED-C) were performed to explore the influence of the interlayers upon the LED optical properties, as shown in Fig. 6. All the LED samples emit at a wavelength around 440 nm. The best PL peak intensity can be observed for LED-C. This is because the SL interlayer can effectively reduce the dislocations density and the probability for dislocations propagating into the MQWs, resulting in better internal quantum efficiency.

After the PL characterization, 300μm × 300μm LED chips on Si were fabricated with LED-B and LED-C, using a standard three-mask process. LED-A was not processed because of the cracks, poor crystalline quality and weak PL intensity. The L-I and I-V characteristics of unpackaged LEDs from samples B and C are shown in Fig. 7. Under a driving current of 20 mA, the forward voltages of LED-B and LED-C were 3.72 V and 3.45 V, respectively. The output power of LED-B and LED-C was measured to be 1.34–1.40 mW and 1.66–1.73 mW, respectively. The average improvement is about 24%. The electroluminescence (EL) characterization results are consistent with the PL results. So it can be concluded that LED performance is enhanced as the GaN crystalline quality is improved by the AlN/GaN SL interlayer.

4. Conclusion

In summary, both stress and crystalline quality of GaN-based LED on Si (111) substrates can be improved with the AlN/GaN SL interlayer. By XRD and Raman characterization, it can be found that AlN/GaN SL interlayer can effectively reduce the dislocation density and improve the stress state. From the PL and EL measurements, it was found that the optical properties of the LEDs were enhanced with the AlN/GaN SL interlayer. Optical output power of LEDs with MT-AlN ML interlayer and AlN/GaN SL interlayer was compared and LEDs with the AlN/GaN SL interlayer were shown to have an average improvement of 24%.

Acknowledgments

The authors would like to thank the Materials Characterization & Preparation Facility and Nanoelectronic Fabrication Facility in the Hong Kong University of Science and Technology for their help in material characterization and device fabrication. This work was supported in part by a grant (GHP/048/11) from the Innovation and Technology Commission (ITC) of Hong Kong Special Administrative Government (HKSAR).

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