Wiley Online Library
Early View publication on www.wileyonlinelibrary.com
(issue and page numbers not yet assigned;
citable using Digital Object Identifier – **DOI**)

Phys. Status Solidi A, 1–5 (2016) / **DOI** 10.1002/pssa.201532803

physica status solidi a
www.pss-a.com
applications and materials science

Optimization of electrode structure for flip-chip HVLED via two-level metallization

Yuefei Cai[**,1], **Xinbo Zou**[**,1,2], **Wing Cheung Chong**[1], **and Kei May Lau**[*,1,2]

[1] Department of Electronic and Computer Engineering, HKUST, Hong Kong
[2] HKUST Jockey Club Institute for Advanced Study, HKUST, Hong Kong

Received 1 October 2015, revised 18 December 2015, accepted 21 December 2015
Published online 25 January 2016

Keywords electrodes, high voltage light-emitting diodes, metallization, solid state lighting

[*] Corresponding author: e-mail eekmlau@ust.hk, Phone: +0852 2358 7049, Fax: +852 2358 1485
[**] These authors contributed equally to this work.

In this article, we demonstrated an optimized electrode structure for high voltage LED (HVLED) using a two-level metallization technique. The first-level metallization is to form interdigitated p and n electrodes with narrow metal fingers. After passivation, a second-level reflective metallization was deposited to form a continuous reflector. Comparing the performance of HVLEDs with bar shape electrode, square shape electrode, and n finger interposed electrode, the HVLEDs with interdigitated p and n finger electrodes show better current uniformity, higher light output power (LOP) and larger wall plug efficiency (WPE). The LOP of such single HVLED chip with 8 sub LED cells on pattern sapphire substrate sample reaches 500 mW at 100 mA current injection. Using flip-chip bonding technique to connect four such chips serially, LOP can reach 2 W at 100 mA drive current. The high brightness HVLED with optimized electrodes enables flexible driver designs for solid state lighting and other applications.

1 Introduction To improve the brightness of GaN light emitting diode (LED) at high-input power conditions, one approach is to increase LED chip size to alleviate the notorious efficiency droop [1]. Another approach is to connect in series a number of LEDs onto a single board or into a single chip and to operate those LEDs in a high voltage low current mode [2–6]. Such an operation mode enables the high voltage LED (HVLED) to achieve higher efficiency than the conventional LED at the same input power density. The high efficiency of HVLED also translates to easier thermal management.

As for the fabrication of HVLED, monolithic integration of several sub LED cells into a single chip is preferred over the multi-chip technology, which is less reliable and more costly. A number of HVLED design and fabrication methods have been explored, including top-emission HVLED [2], thin-film HVLED [3–5], and flip-chip HVLED [6]. It has been reported that cell and electrode design plays a key role in determining the device performance [7, 8]. For example, in top-emitting LEDs, from which light is extracted from the p-type GaN epilayers, electrodes are typically designed to cover a minimum area to maximize light extraction [9–11]. For the flip-chip LED structure, however, light is reflected by the reflective metal layer on the p-side and extracted from the inverted sapphire substrate. One of the methods is to design the p electrode metal covering the whole region of LED mesa since it functions as both electrical conduction and optical reflection [12–18]. In this way, the light emission can be effectively reflected as the reflective p electrode covers the same area of the emission region. Although the optical loss can be kept to be minimum, but there is still much room to improve the electrical performance, especially the current crowding effects and non-uniformity distribution of electric field.

One improvement made by Ochiai et al. [18] was to increase the number of n contact fingers. By increasing the number from 4 to 8, the current spreading became more uniform. However, increasing the number of n contact fingers also leads to a loss in the effective light emission area as more of the active region will be etched for n contact finger formation.

In this article, we report an optimized p-electrode structure using a two-level metallization technique. The first-level metallization is to form interdigitated p and n electrodes with narrow metal fingers. After passivation, optical reflection is then achieved by using a second-level metallization, in which metal covers the entire LED surface and forms a continuous light reflector. In this way, good current spreading and light extraction can be obtained at the same time.

2 Device design and fabrication

2.1 Device design We design four types of structures for light out power (LOP) and wall plug efficiency (WPE) comparison purpose. The four types of structures are interdigitated p and n finger electrode, n finger interposed electrode, square-shaped electrode and bar-shaped electrode, as shown in Fig. 1(a–d), respectively. The interdigitated electrodes and surrounding n-electrodes were reported to be effective in getting low series resistance in LEDs [15–20].

The four types of HVLED chips labelled structure A (interdigitated PN finger), B (N finger), C (square shape), and D (bar shape) have the same chip size ($560 \times 570\ \mu m^2$) but slightly different effective light emission areas (mesa sizes). The effective areas for structures A, B, C, and D are 0.28, 0.28, 0.27, and 0.29 mm^2 due to their different mesa shapes. In structure A, the distance between the p and n electrode is designed to be 80 μm, which is far smaller than the calculated current spreading length (200–300 μm depending on the p-GaN layer resistivity and thickness) according to Guo's model [15].

The difference between structure A and structure B lies in the shape and area of the p electrode, as shown in Fig. 1(e). For structure A, the p-electrode was made up of 10 μm-wide narrow metal lines (only 1/15 of the mesa area) whereas the p-electrode of structure B covers the whole p-type GaN mesa region. To realize the flip-chip LED design, the p electrode metal of the HVLED in structure B also serves as the reflective mirror, whereas in structure A, a two-level metallization technique is used in the fabrication.

The structure C is similar to the structure B, in which p electrode metal covers most of the mesa region to aid current spreading on p-GaN and also to serve as reflective mirror. But the n contact configuration of structure B with n interposed finger is different from structure C with n electrode surrounding the mesa. The structure D is similar to the structure A, where p electrode only serves as current spreading purpose and a second level metallization is used to achieve light reflection. But the n contact configuration of structure A with n interposed finger is different from structure D with n electrode on one side of the mesa.

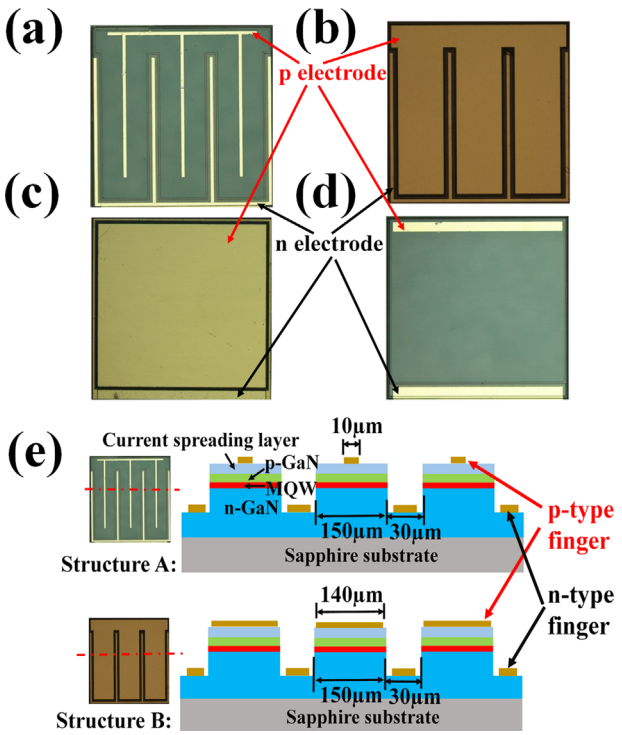

Figure 1 Four types of electrode patterns for sub-LED cells of HVLEDs after first-level metallization. (a) Structure A: interdigitated PN finger; (b) structure B: N finger; (c) structure C: square shape; (d) structure D: bar shape; and (e) cross section comparison between structures A and B.

2.2 Device fabrication The HVLED fabrication process started from a 2 in. GaN LED wafer grown on a planar sapphire substrate. After isolation trench etching, mesa definition and current spreading layer deposition, the first-level metallization was done, and 2 nm/200 nm/50 nm/50 nm Cr/Al/Ti/Au was deposited as the p and n electrodes. After this, individual sub LED cells were formed. The shapes of the four types of sub LED cells are shown in Fig. 1. Subsequently, a passivation layer was deposited and contact holes were opened. The second-level metallization, which consists of a stacking layer of 2 nm/200 nm/50 nm/80 nm Cr/Al/Ti/Au metal, was deposited to interconnect the individual LED sub cells into a whole HVLED chip as well as to act as a highly reflective layer. Then, the sapphire substrate was thinned down, polished, and the wafer was diced into HVLED chips. Finally, the chips were flip-chip bonded onto a silicon submount to extract light from the thinned sapphire substrate side.

Figure 2(a) displays an optical photograph of a fabricated HVLED with structure A. It consists of 8 sub LED cells connected in series. Current flows from the p bonding pad into the first sub LED cell, named C1, to C2 . . . C7, and C8, finally flowing out from the n bonding pad. In fact, the number of sub LED cells of an HVLED chip can be flexibly adjusted to 11, 16, or even more, for different voltages or power applications. Figure 2(b) is an SEM image showing the details of cell-to-cell connection. Figure 2(c) illustrates two adjacent sub LED cells interconnected by using the two-level metallization technique. The sandwich

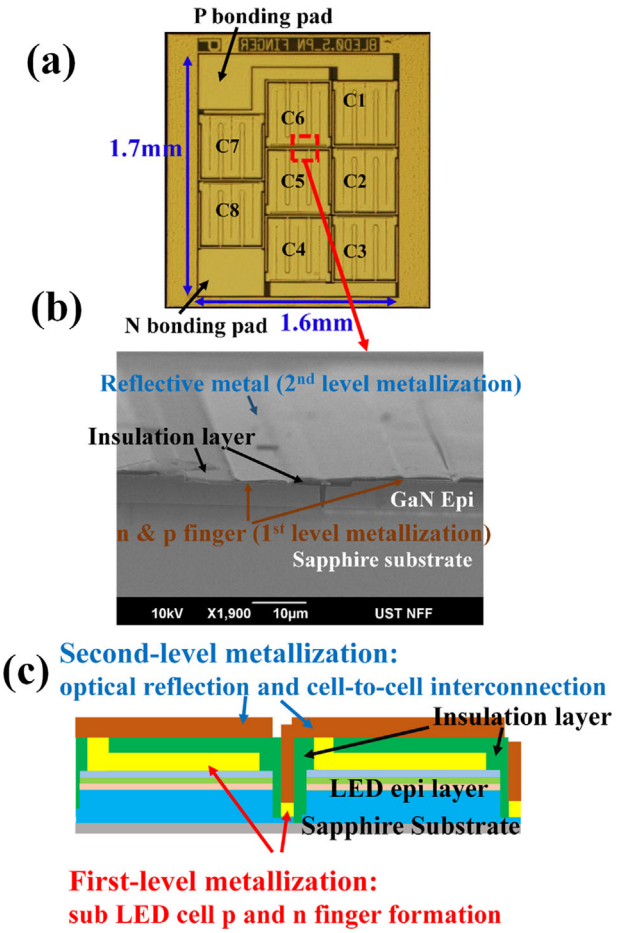

Figure 2 (a) HVLED chip microscope image, (b) SEM image of the sub LED cell to cell interconnection. (c) Cross section of the HVLED chip by two-level metallization.

structure consists of first-level metallization (for individual sub LED cell p and n finger electrode formation), an insulation layer (for trench filling and sidewall passivation) and second-level metallization (either for optical reflection or for sub LED cell-to-cell interconnection). Here, transparent curable polymer is used as the insulation layer to avoid electrical short of the p and n region and to guarantee minimum light absorption by the passivation polymer.

HVLED chips consisting of sub LED cells with other types of electrode patterns such as structures B, C, and D were also fabricated using the same methods mentioned here.

3 Measurement

3.1 *I–V* characterization The *I–V* characteristic in Fig. 3 shows that the HVLED with structure B (n finger interposed electrode) has the lowest forward voltage at 20 mA. This can be explained by the very short distance between the p and n fingers resulting from the coverage of the p electrode metal on the whole mesa top. In addition, the interposed n finger electrode helps to achieve a uniform

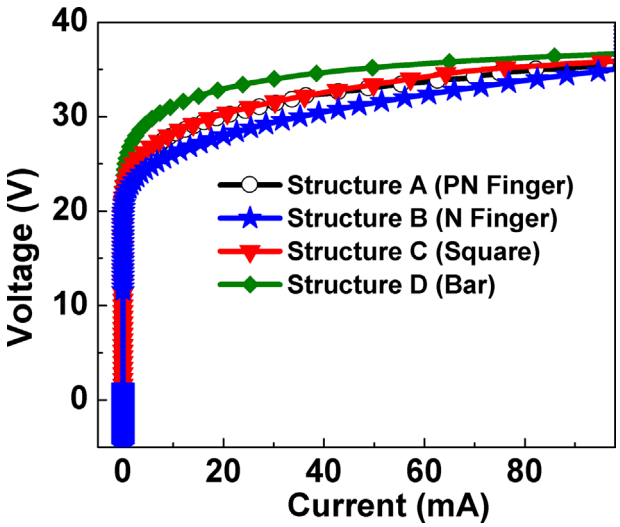

Figure 3 Current–voltage characteristic of four types of HVLED chips with 8 sub LED cells.

current density. For the HVLED chip with structure D (bar shaped electrode), the forward voltage is larger than the one with structure A (interdigitated PN finger electrode) and structure C (square shaped electrode). This poor current spreading in D resulted from its large p and n electrode distance and large p-type GaN resistance (with no metal covering on it).

To further explore the current spreading performances of these four types of HVLED chips, current density distribution at 100 mA current injection across the whole mesa region was simulated by SpeCLED software, which is shown in Fig. 4 and Table 1.

From the simulation results, we can see that structure A (interdigitated PN finger electrode) has the best current spreading performance among the four types of structures. Comparing with structure B, the structure A (interdigitated PN finger electrode) can spread current more evenly than structure B (N finger electrode). This can be explained by the current spreading model given in [15]. By shrinking the

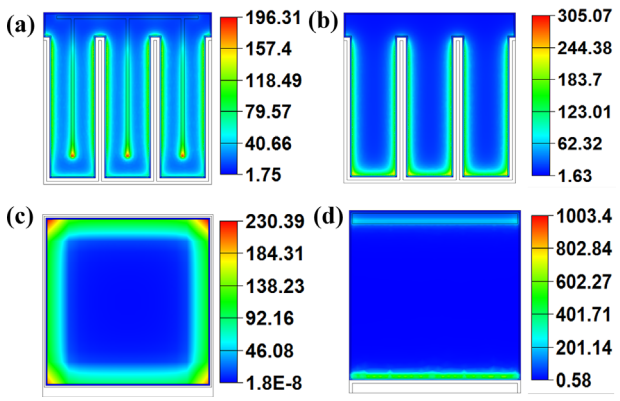

Figure 4 Simulated current density distribution at 100 mA current injection for different electrodes; (a) structure A, (b) structure B, (c) structure C, and (d) structure D.

Table 1 Simulated current density and its RMS value at 100 mA.

electrode pattern	A (PN finger)	B (N finger)	C (square)	D (bar)
average current density ($A\,cm^{-2}$)	39.6	39.6	36.5	34.8
maximum current density ($A\,cm^{-2}$)	196.3	305.1	230.4	1003.4
root-mean-square value ($A\,cm^{-2}$)	47.8	57.1	60.3	116.2

140 μm-wide p electrode metal into 10 μm-wide metal line, resistance in p cladding layer will be increased. Keeping the n-side resistance the same, the increase of p-side resistance will make the current spreading length even longer, thus better current spreading can be obtained. The improvement in current spreading also can be seen from the comparison of Fig. 4(a) with (b) at 100 mA current injection.

3.2 Optical emission In order to compare the light emission uniformity of different electrode patterns design, the optical emission of the four types of HVLED chips were flip-chip bonded on the same types of silicon submount and measured by a calibrated CCD camera at different current injections (20, 50, and 100 mA). Optical intensities at different injection currents have been normalized by the CCD integration times for comparison.

As shown in Fig. 5, the HVLED with structures C and D cannot emit very uniform light even at low-current injection (20 mA). The light emission uniformity becomes more uneven and congregates near the electrode region at higher injection current, which is caused by the current crowding phenomenon. From Fig. 5(d), a current spreading length of 256 μm was extracted, which is consistent with the theoretical calculation results in the beginning of Section 2. For the HVLED with structure B (N finger electrode), very uniform light can be obtained at low-current injection, but light emission becomes non-uniform and congregates near the n-type electrode region when current is increased to 50 mA. This current crowding phenomenon becomes more obvious at 100 mA, as shown in Fig. 5(b). Most of the optical intensity peak values are concentrated near the boundary of p and n electrode. For the HVLED with structure A (interdigitated PN finger electrode), light emission is still very uniform even when current increases to 100 mA. This indicates good current spreading ability of this type of electrode compared with the structure B and the other two types of electrodes.

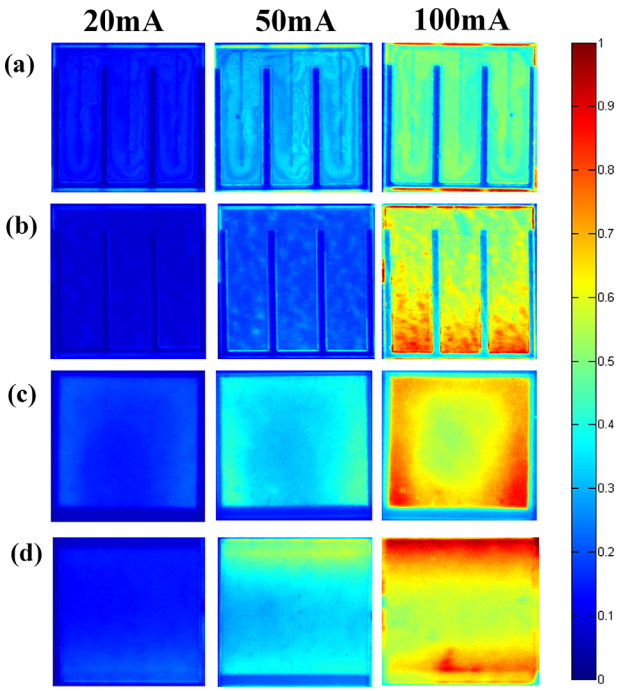

Figure 5 Optical emission uniformity comparison at 20, 50, and 100 mA for the sub LED cells on HVLED with different electrode patterns; (a) structure A (interdigitated PN finger electrode), (b) structure B (N finger electrode), (c) structure C (square-shaped electrode), and (d) structure D (bar-shaped electrode).

3.3 LOP and WPE measurement To compare the light output power (LOP), four types of HVLED chips with 8 sub LED cells were flip-chip bonded onto the same types of silicon submount. It should be noted that all the HVLED chips were fabricated on the same planar substrate sapphire wafer, without any roughening or encapsulation.

Shown in Fig. 6, structures A and D with two-level metal layers sandwiched by a passivation layer, exhibit higher LOP than structures B and C, which directly use electrodes as reflectors. This confirms the effectiveness of our two-level metallization design in achieving higher optical power. Although structure D has slightly higher LOP than structure A for injection current smaller than 60 mA, the larger forward voltage and early LOP saturation hinder practical applications of structure D. With increase of injection current, the LOP of structure A increases almost

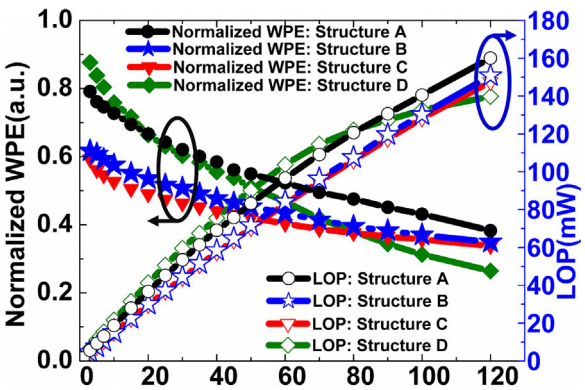

Figure 6 Light output power and wall plug efficiency of four types of HVLED chips with different electrode designs.

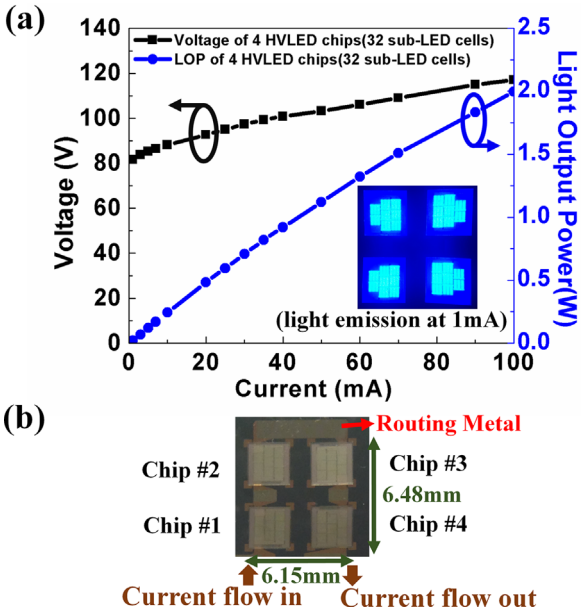

Figure 7 Flip-chip HVLED (a) LIV curve (inset: light emission at 1 mA), (b) HVLED chips bonded on a silicon submount.

linearly at injection current up to 120 mA. Benefiting from its relatively low-forward voltage, structure A shows the highest WPE for current larger than 20 mA among the four samples. Comparing with the HVLED chips with structures B, C, and D, the HVLED chip with structure A has 5.6%, 9.2%, and 17.3% improvement in WPE at 100 mA. This improvement can be attributed to more uniform current spreading of structure A especially at high current injection.

Based on the above experiment and analysis, the HVLED chip consisting of 8 sub LED cells with interdigitated finger-shaped electrode was fabricated on a patterned substrate sapphire wafer. By transferring the fabrication from planar sapphire substrate sample to patterned sapphire substrate sample, the LOP of a single chip reaches to 500 mW at 100 mA current injection. After flip-chip bonding of four such chips onto one silicon submount with series electrical connection, the light output power and light emission were measured. The LOP can reach up to 2 W at 100 mA current injection, as shown in Fig. 7. Further enhancement of efficiency could be expected by utilizing surface roughening and silicone encapsulation.

4 Conclusions An optimized interdigitated p and n finger electrode was designed and fabricated for flip-chip HVLED chips to achieve good current spreading and high light output power. The current spreading of this electrode pattern was analyzed and compared with bar shaped, square shaped, and n finger interposed electrodes. Our optimized interdigitated p and n finger electrode can achieve the highest efficiency and light output power among the four due to good current spreading even at high current injection. The HVLED chip with a total 32 sub LED cells can emit 2 W at 100 mA current injection without roughening or encapsulation, which enables it to be a good candidate for solid state lighting applications with flexible driver designs.

Acknowledgements This work was supported by the Research Grants Council of the Hong Kong Special Administrative Region Government under the Theme-Based Research Scheme (Grant T23-612/12-R). The authors would like to thank Spec LED Research Group for the simulation support. Also thanks to Zhang Yu for the generous help in light emission measurement, as well as to the staff of the MCPF & NFF of HKUST for their technical support.

References

[1] S. Pimputkar, J. S. Speck, S. P. DenBaars, and S. Nakamura, Nature Photon. **3**(4), 180 (2009).
[2] T. Zhan, Y. Zhang, J. Ma, T. Tian, J. Li, Z. Q. Liu, and X. Y. Yi, Photon. Tech. Lett. **25**(9), 844 (2013).
[3] M. L. Tsai, J. H. Liao, J. H. Yeh, T. C. Hsu, S. J. Hon, T. Y. Chung, and K. Y. Lai, Opt. Express **22**(22), 27102 (2013).
[4] C. H. Tien, K. Y. Chen, C. P. Hsu, and R. H. Horng, Opt. Express **22**(106), A1462 (2014).
[5] M. L. Tsai and K. Y. Lai, Appl. Phys. Express **7**(2), 022103 (2014).
[6] Y. C. Chiang, B. C. Lin, K. J. Chen, S. H. Chiu, C. C. Lin, P. T. Lee, M. H. Shih, and H. C. Kuo, Int. J. Photoenergy **2014** (2014), 385257 (2014).
[7] C. H. Wang, D. W. Lin, C. Y. Lee, M. A. Tsai, G. L. Chen, H. T. Kuo, and G. C. Chi, IEEE Electron Device Lett. **32**(8), 1098 (2011).
[8] S. Li, K. T. Lam, W. C. Huang, and S. J. Chang, J. Photon. Energy **5**(1), 057605 (2015).
[9] Y. B. Tao, S. Y. Wang, Z. Z. Chen, Z. Gong, E. Y. Xie, Y. J. Chen, B. R. Rae, R. H. Henderson, and G. Y. Zhang, Phys. Status Solidi C **9**(3–4), 616 (2012).
[10] B. Cao, S. M. Li, R. Hu, S. J. Zhou, Y. Sun, and Z. Y. Gan, Opt. Express. **21**(21), 25381 (2013).
[11] G. J. Sheu, F. S. Hwu, J. C. Chen, J. K. Sheu, and W. C. Lai, J. Electrochem. Soc. **155** (10), H836 (2008).
[12] D. A. Steigerwald, S. D. Lester, and J. Wierer, jr., US Patent 6,573,537.2003-6-3.
[13] H. Rodríguez, N. Lobo, S. Einfeldt, A. Knauer, M. Weyers, and M. Kneissl, Phys. Status Solidi A **207**(11), 2585 (2010).
[14] F. S. Hwu, T. H. Sung, C. H. Chen, J. W. Tseng, H. Qiu, and J. C. Chen, IEEE Photon. J. **5**(2), 6600515 (2013).
[15] X. Guo, Y. L. Li, and E. F. Schubert, Appl. Phys. Lett. **79**(13), 1936 (2001).
[16] K. Y. Chen, C. H. Tien, C. P. Hsu, C. Y. Pai, and R. H. Horng, IEEE Trans. Electron Devices **61**(12), 4128 (2014).
[17] J. J. Wierer, D. A. Steigerwald, M. R. Krames, J. J. O'Shea, M. J. Ludowise, G. Christenson, Y. C. Shen, C. Lowery, P. S. Martin, S. Subramanya, W. Götz, N. F. Gardner, R. S. Kern, and S. A. Stockman, Appl. Phys. Lett. **78**(22), 3379 (2001).
[18] W. Ochiai, R. Kawai, A. Suzuki, M. Iwaya, H. Amano, S. Kamiyama, and I. Akasaki, Phys. Status Solidi C **6**(6), 1416 (2009).
[19] X. Guo and E. F. Schubert, Appl. Phys. Lett. **78**(21), 3337 (2001).
[20] K. M. Lau, K. M. Wong, X. Zou, and P. Chen, Opt. Express **19** (104), A956 (2011).