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Relaxation kinetics of interface states and bulk traps in atomic layer deposited $ZrO_2/\beta\text{-Ga}_2O_3$ metal-oxide-semiconductor capacitors

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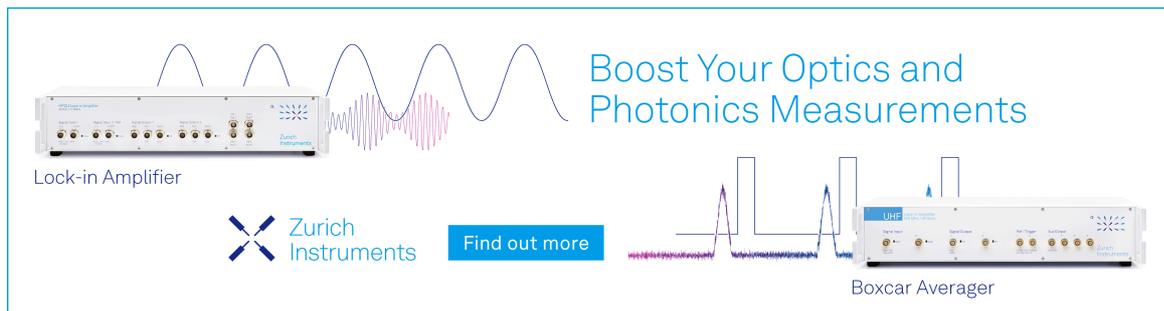


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ABSTRACT

The study of interface states and bulk traps and their connection to device instability is highly demanded to achieve reliable $\beta\text{-Ga}_2\text{O}_3$ metal-oxide-semiconductor (MOS) devices. However, a comprehensive analysis of the capture/emission behavior of interface states and bulk traps can be challenging due to widespread time constant distribution. In this study, using capacitance transient measurement tools, trap states of the $\text{ZrO}_2/\beta\text{-Ga}_2\text{O}_3$ MOS gate stack were explicitly investigated, particularly its bias- and temperature-dependent relaxation kinetics. As forward bias is enlarged, it is observed that the interface state density (D_{it}) increases by 12.6%. Two bulk traps with discrete levels identified as 0.43 eV (E1) and 0.74 eV (E2) below the conduction band minimum were extracted by deep-level transient spectroscopy. It is further revealed that the emission processes of E1 and E2 are thermally enhanced, while the capture processes remain insensitive to temperature. The electric-field dependence of E1 indicates that the dominant mechanism follows the rule of Poole-Frenkel emission. The capacitance-voltage (C-V) hysteresis deteriorated at a higher forward bias due to the higher trap density and increased population of trapped charges. These findings provide an important framework for future device optimization to improve the reliability and performance of $\beta\text{-Ga}_2\text{O}_3$ MOS devices.

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I. INTRODUCTION

Beta-gallium oxide ($\beta\text{-Ga}_2\text{O}_3$) has attracted considerable attention for high power and radiation-hard applications owing to its large bandgap (4.9 eV), high critical breakdown field strength (E_{BR}) of 8 MV/cm, and high Baliga Figure-of-Merit (BFOM).¹⁻³ A variety of dielectrics have been employed in fabricating Ga_2O_3 -based metal-oxide-semiconductor field effect transistors (MOSFETs), including SiO_2 ⁴ and high-permittivity (k) dielectrics such as Al_2O_3 ,^{5,6} HfO_2 ,⁷ ZrO_2 ,⁸ and HfAlO ⁹ by atomic layer deposition (ALD). Recently, normally off $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ MOSFETs with outstanding kV-level breakdown voltage have also been demonstrated.¹⁰

Despite the dramatic improvement seen in the electrical properties of $\beta\text{-Ga}_2\text{O}_3$ MOS devices, some reliability issues still remain

open, including gate leakage, the capacitance-voltage (C-V) hysteresis phenomenon, flatband voltage (V_{FB}) shift, DC-RF dispersion, and premature breakdown.¹¹⁻¹⁴ It is widely accepted that interfacial states and bulk traps are crucial in determining the performance and stability of Ga_2O_3 MOS devices.¹⁵ Several reports have studied the bias-dependent threshold voltage instability in lateral $\beta\text{-Ga}_2\text{O}_3$ MOSFETs^{5,16} and vertical Fin-MOSFETs.¹⁷ This phenomenon has been ascribed to the capturing/releasing processes of trap states upon positive and negative bias. Therefore, it is demanding to deposit a high-quality dielectric layer with minimum number of trap states and to accurately evaluate the trap density and energy distribution.

Some reports have investigated the energy distribution of defect state in MOS structures including both interface state

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continuum and discrete energy levels.^{18–20} The density of interface states (D_{it}) of SiO_2 , Al_2O_3 , HfO_2 , HfAlO , and AlSiO on $\beta\text{-Ga}_2\text{O}_3$ MOS capacitors (MOSCAPs) have been previously analyzed by quasi-static C–V,⁴ photo-assisted C–V,^{5,11} the Terman method,²¹ the Hi–Lo method,⁹ and deep-level transient spectroscopy (DLTS).^{22,23} Most studies mainly focus on the density of state continuum, whereas the analysis of trap with discrete-level properties is limited.^{22,24} Meanwhile, the density and distribution of interface states in $\text{ZrO}_2/\beta\text{-Ga}_2\text{O}_3$ are still lacking. ZrO_2 has emerged as a promising gate dielectric material for Ga_2O_3 MOS devices with a conduction band offset (ΔEc) of 1.2 eV and a high dielectric constant,⁸ resulting in its ability to achieve lower leakage current and a lower effective oxide thickness, respectively.^{1,25}

Furthermore, it is demanding to comprehensively understand the kinetics of releasing/capturing nonequilibrium carriers by trap states in MOS-based device, which are fundamental to mitigation of trap-induced degradation and time-dependent variability phenomena.²⁶ However, by the conventional conductance method, identifying the bias- and temperature-dependent emission/capture kinetics of interface states can be challenging due to the broad energy distribution.^{27,28} The conduction loss was not detected in the measured frequency range (e.g., 1 kHz–5 MHz) due to the extremely long time constant associated with the deep energy level, leading to the inaccurate calculation of D_{it} . Capacitance-based DLTS^{29,30} holds the advantage of identifying a wide range of time constants for trap states by varying the temperature and pulse bias. Thus, quantitative assessment of trapping/detrapping processes associated with a specific trap state would be enabled. To the best of our knowledge, bias-temperature instability (BTI) and C–V hysteresis of the $\beta\text{-Ga}_2\text{O}_3$ MOS gate stack and related relaxation kinetics of trap states remain to be clarified yet, particularly at low temperatures. Without knowledge of these trap states, it is hard to establish insights for improvement of the interfacial quality of the dielectric/ $\beta\text{-Ga}_2\text{O}_3$ and device performances.

In this work, the properties of interface states and bulk traps of ALD-deposited ZrO_2 on $(\bar{2}01)$ oriented n -type $\beta\text{-Ga}_2\text{O}_3$ MOS capacitors were investigated by C–V methodologies and capacitance-based deep-level transient spectroscopy (DLTS). The influence of injection pulse bias and temperature on the distribution and transient response of interface states was demonstrated with three-dimensional (3D) transient mapping. Two bulk traps E1 and E2 with a discrete energy level within Ga_2O_3 were revealed by temperature-scan DLTS and isothermal capacitance transient spectroscopy (ICTS) measurements, respectively. The possible origin of these two trap levels was also discussed. The electrical signatures including C–V stretch-out and hysteresis-related defect states of $\beta\text{-Ga}_2\text{O}_3$ MOS devices have been investigated. This study provides a guideline for the analysis of relaxation kinetics of interface states in a wide range of Ga_2O_3 MOS structures, thereby enhancing device reliability and performance.

II. EXPERIMENTAL DETAILS

A. Sample preparation

Figure 1(a) illustrates a fabricated vertical device schematic of an n -type $(\bar{2}01)$ $\beta\text{-Ga}_2\text{O}_3$ MOS capacitor with a ZrO_2 gate dielectric. The thickness of the ZrO_2 layer was measured as 30 nm using

an ellipsometer. Square top contacts, with a side length of $150\ \mu\text{m}$, were formed by $\text{Ti}/\text{Au} = 30/100$ nm. The backside Ohmic contact was formed by $\text{Ti}/\text{Al}/\text{Ni}/\text{Au} = 15/80/20/60$ nm. After deposition, samples were processed by rapid thermal annealing (RTA) in N_2 at $700\ \text{C}$ for 40 s.

B. Capacitance transient measurement

The waveform of gate bias for capacitance transient measurement in MOSCAPs is plotted in Fig. 1(b). The rectangular pulse bias (V_p) with pulse durations (t_p) was set to fill the trap states. Subsequently, after the waiting time (t_0), the applied bias was turned to the measured bias (V_m), resulting in the transient release of trapped electrons within the measurement time window (T_m) for measurement. Consequently, the alteration of trapped charges located in proximity to the MOS interface can be observed via a capacitance transient, which was evaluated as a function of measurement time. In Fig. 1(c), the time-dependent capacitance transient ($\Delta C - t$) measurements were conducted to monitor the emission processes of trap states in T_m from t_1 (10 ms) to t_2 (1000 ms) at 300 K. The transients were obtained by keeping the pulse bias at 1 V, but with varying pulse durations from 128 ns to 1 s. Interface states exhibit a widespread effective response time constant (τ_{eff}) due to their continuous energy distribution and can be represented as the sum of n ideal exponential decays using the extended-Debye model,^{31–33}

$$\Delta C(t) = \sum_{i=1}^n \Delta C_i \times \exp\left(-\frac{t}{\tau_{effi}}\right) \approx |\Delta C_0| \exp\left\{-\left(\frac{t}{\tau_{eff}}\right)^\beta\right\}, \quad (1)$$

where ΔC_0 is the total change of transient capacitance amplitude and ΔC_i and τ_{effi} are the amplitude and time constants of each process, respectively. β is the stretched-exponential factor ($0 < \beta \leq 1$) of the response time. For each transient, the extracted parameters by Eq. (1) have been summarized in Table I. The closer β approaches zero, the more transient decay deviates from the monoexponential, implying that the relaxation processes stem from superposition of multiple exponential emissions.^{27,34} As the pulse duration was increased from 128 ns to 1 s, τ_{eff} shows a reduction from 0.73 to 0.38 s. The corresponding increase in ΔC with elevating t_p suggests the existence of more trapped charges by trap states. However, when t_p exceeded 10 ms, both β and ΔC exhibited negligible changes, owing to complete occupation of trap states by injected carries.

III. RESULTS AND DISCUSSION

Figure 2(a) illustrates the bidirectional C–V characteristics at 1 MHz. This stretch-out phenomenon in C–V curves has been observed in other $\beta\text{-Ga}_2\text{O}_3$ MOSCAPs, suggesting the existence of trap states, which may include interface states and bulk traps.^{4,35} The higher density of the interface state will result in a more pronounced stretch-out phenomenon.³⁶ The possible reason for rising accumulation capacitance is the filling of the interface state or border traps when the MOSCAP is in accumulation.¹⁸ As indicated in Fig. 2(b), the $1/C^2 - V$ curve was plotted at 300 K. The frequency

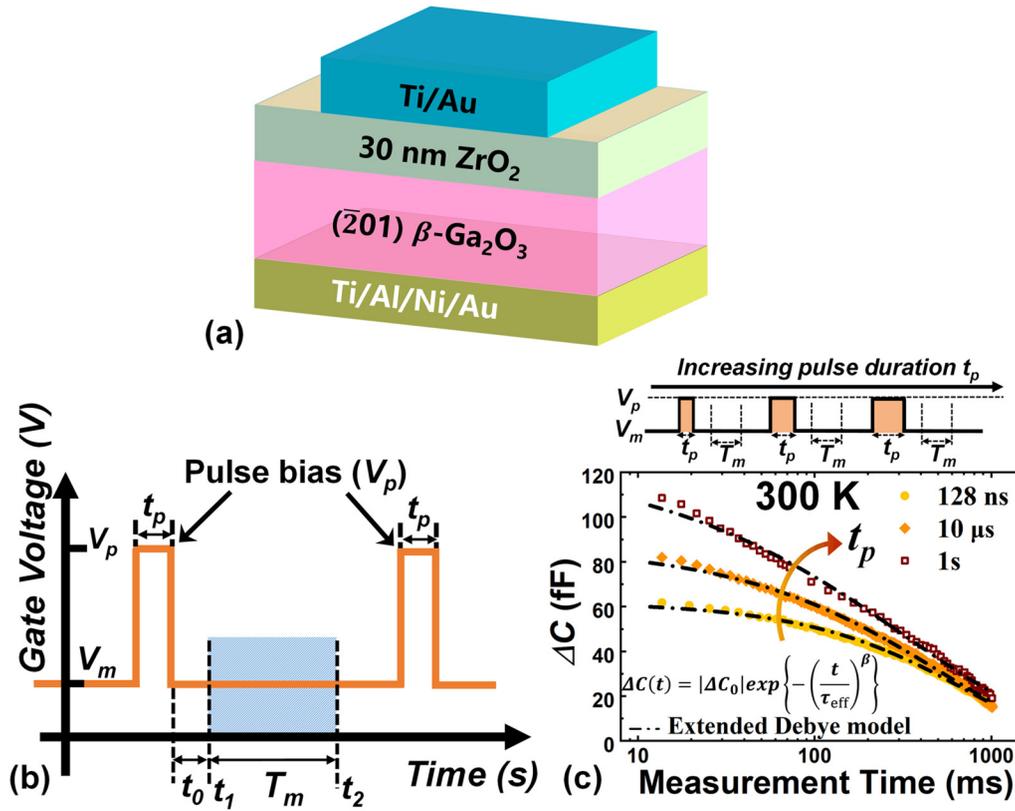


FIG. 1. (a) Schematic of $ZrO_2/\beta\text{-Ga}_2O_3$ (201) MOSCAPs. (b) The waveform of gate bias. (c) Schematic with various pulse durations (t_p) and the inverted capacitance transient of the emission process with t_p .

and AC amplitude of the C–V test were 1 MHz and 50 mV, respectively. The doping concentration (N_s) was calculated as $9.0 \times 10^{16} \text{ cm}^{-3}$ from the slope of $1/C^2$ –V, according to $N_s = \frac{2 \cdot d(V)}{q \epsilon_s \epsilon_0 A^2 d(C^{-2})}$, where q is the element charge, ϵ_0 is the vacuum permittivity, ϵ_s is the relative dielectric constant of $\beta\text{-Ga}_2O_3$, and A is the area of MOSCAPs.

Figure 2(c) illustrates the impact of forward bias stress on MOSCAP stability by means of step-stress C–V measurements conducted at room temperature.^{11,37} In the bidirectional C–V loop, the bias was incrementally swept upward from –10 to 5 V as a reference curve. Subsequently, the bias was immediately swept backward from the maximum gate bias ($V_{g,max}$) to –10 V. $V_{g,max}$ was varied

from 1 to 5 V by steps of 1 V during the downward sweep. As $V_{g,max}$ increased, it is observed that the deviation from reference upward C–V became more pronounced, and the hysteresis width enlarged. The hysteresis width of C–V curves was determined from the variation between the initial upward sweep and downward sweep curves at different $V_{g,max}$ using 110 nF/cm² as the criterion. Figure 2(d) illustrates that the value of hysteresis width ranged from 0.20 to 2.01 V as $V_{g,max}$ increased from 1 to 5 V. This trend suggests a significant enhancement of C–V hysteresis at larger positive bias, which is attributed to a higher trap density.

In Fig. 3(a), the continuum distribution of interface state density was extracted from DLTS measurement by varying different filling pulse bias from 0.1 to 1.2 V. This method can well reveal temperature and bias dependency D_{it} at the ZrO_2/Ga_2O_3 interface. Deep interface states with long time constants of several seconds or above, which cannot respond to AC signal in conventional conduction method, can still be detected and calculated. The amplitude of D_{it} is proportional to the DLTS signal amplitude (b_1), and the relationship is as follows:^{27,38}

$$D_{it} = \frac{\epsilon A N_s C_{ox} b_1}{k T C_M^3 \ln(t_2/t_1)}, \quad (2)$$

TABLE I. Extracted parameters from the capacitance transient upon applying various pulse durations using the extended-Debye model.

Pulse duration (t_p)	128 ns	1.5 μ s	10 μ s	10 ms	1 s
τ_{eff} (s)	0.73	0.53	0.51	0.42	0.38
β	0.75	0.73	0.63	0.57	0.53
ΔC (fF)	63	82	85	115	116

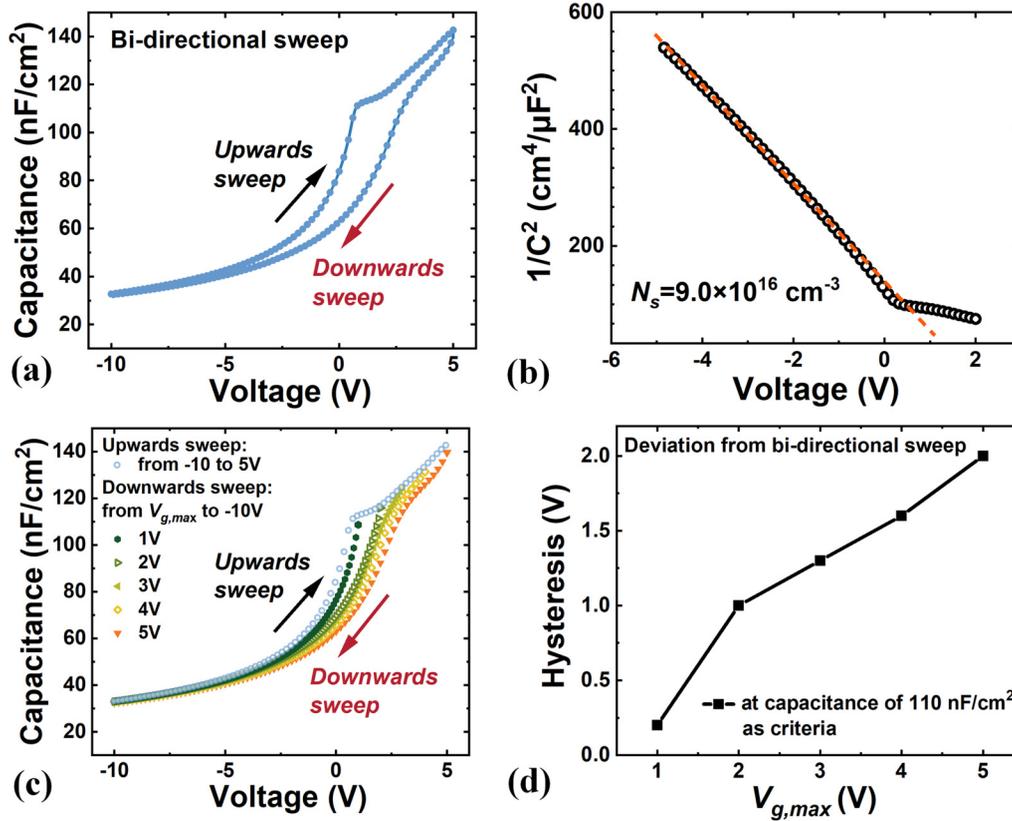


FIG. 2. (a) Bidirectional sweep C–V characteristics at 1 MHz. (b) The $1/C^2$ –V curves of MOSCAPs. (c) Bidirectional C–V characteristics by upward sweep as the reference curve and then downward sweep from various $V_{g,max}$ to -10 V. (d) Extracted C–V hysteresis width as a function of $V_{g,max}$ from (c).

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where $\epsilon = \epsilon_s \epsilon_0$, C_{ox} is the capacitance of the oxide layer, C_M is the capacitance at the measured voltage V_m , k is the Boltzmann constant, T is the temperature, and t_2 and t_1 are the chosen measurement and sampling times. The corresponding activation energy $E_C - E_T$ could be written as

$$E_C - E_T = kT \ln(v_{th} N_C \sigma_n \tau_e), \quad (3)$$

where N_C is the effective density state of electrons, τ_e is the emission time of the interface state, and σ_n is the capture cross section of the interface state with a typical value of $1 \times 10^{-15} \text{ cm}^2$.^{35,39}

The distribution of D_{it} covers a continuous energy range from 0.1 to 0.7 eV below the conduction band. Upon applying a pulse bias of 1.2 V, it can be observed that D_{it} drops from $2.63 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at $E_C - 0.40 \text{ eV}$ to a minimum value of $2.29 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at $E_C - 0.16 \text{ eV}$. The value of D_{it} for $\text{ZrO}_2/\text{Ga}_2\text{O}_3$ is comparable to or even lower than those reported for other dielectrics such as SiO_2 , Al_2O_3 , HfO_2 , and $(\text{Y}_{0.6}\text{Sc}_{0.4})_2\text{O}_3$ by ALD, implying that ALD ZrO_2 has a great potential in high-performance MOS devices.^{21,35,40,41} The continuous interval of activation energy of interface states is consistent with observed stretched-exponential transients in Fig. 1(c). In Fig. 3(b), the pulse

bias and the corresponding electrical-field-dependent activation energy of peak signals have been evaluated. As V_p is elevated, the peak position shifts to lower temperatures, and the activation energy ($E_C - E_T$) of the trap emission process decreased from 0.50 eV at 0.1 V (0.33 MV/cm) to 0.39 eV at 1.2 V (0.4 MV/cm), suggesting that trapped carriers require less energy to overcome the potential barrier and emit at higher fields. With an increase in pulse bias, the maximum value of D_{it} also increased by 12.6%, indicating more injection of carriers induced by the forward bias. In Fig. 3(c), the integration of D_{it} with respect to $E_C - E_T$ yields total charge densities (Q_{it}) trapped by the interface state ranging from 2.99×10^{11} to $7.32 \times 10^{11} \text{ c/m}^2$ with elevating V_p , indicating that the greater occupation level of interface states by carriers and the trapping effect of electrons was enhanced by the forward bias. These values were approximately one order of magnitude lower than those reported Q_{it} of $(1 - 4) \times 10^{12} \text{ C/cm}^2$ for $\text{SiO}_2/\beta\text{-Ga}_2\text{O}_3$ ²² and $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$.³⁹

In Figs. 3(d)–3(f), the three-dimensional transient mapping of the interface state emission process from 70 to 300 K is demonstrated with different V_p of 0.1, 1.0, and 1.2 V. The hump around 175–250 K in the mapping indicated that the charging states are changed by the bulk trap with the discrete level.¹⁸ During the

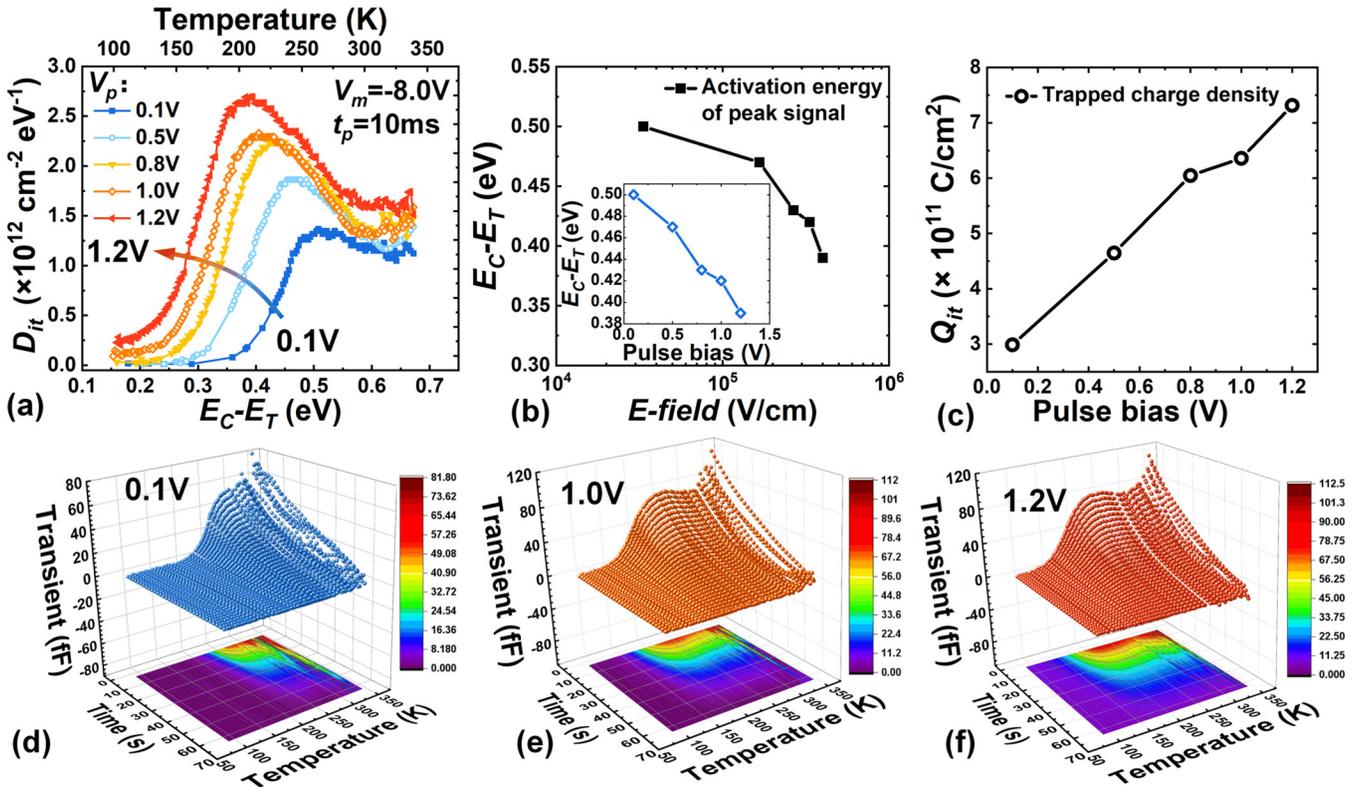


FIG. 3. (a) Distribution of D_{it} extracted from DLTS analysis with various pulse bias V_p over the activation energy. (b) Extracted electrical-field-dependent activation energy of the peak signal from (a). Inset: V_p -dependent energy depth of the peak signal. (c) Extracted bias-dependent trapped charge densities (Q_{it}) of the interface state. 3D mapping of the capacitance transient of interface states at various V_p of (d) 0.1, (e) 1.0, and (f) 1.2 V with measured color map and projection of transient amplitude.

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emission of carriers from interface states, the capacitance transients follow a logarithmic-like decay composed of plenty of overlapping exponential transients. Applying a higher forward bias increases the integral transient amplitude, which is proportional to D_{it} . This augmentation is evident in the maximum value of transient amplitude, which increases from nearly 80 fF at 0.1 V in Fig. 3(d) to 113 fF at 1.2 V in Fig. 3(f). This phenomenon is likely due to the enhanced trapping of interface states by the aid of a higher electric field.

Figure 4(a) displays the temperature scanning of DLTS spectra measured with V_p varying from 0.1 to 1.2 V. Each temperature sweep was carried out by interval steps of 2 K. The pulse duration and V_m were set as 100 ms and -8 V, respectively. The lower temperature part of the DLTS spectrum around 200 K shows a single peak as shown in the shadow region, labeled as a bulk trap E1. This peak is consistent with the distinct peak around 200 K, indicating that the bulk traps originate from specific atomic bonding or mobile charges.^{18,22} When a higher pulse bias is applied, the amplitude of the bulk trap E1 signal becomes enlarged, which is consistent with the observed high-density signal peak in Fig. 3(a).

As shown in Fig. 4(b), the activation energy of E1 was 0.43 ± 0.03 eV with an average value of the capture cross section

(σ_n) of $1.35 \times 10^{-14} \text{ cm}^2$ at V_p of 1 V extracted by Arrhenius analysis, as given by⁴²

$$\ln(\tau_e T^2) = \frac{E_C - E_T}{kT} - \ln(\gamma \sigma_n), \quad (4)$$

where τ_e is the electron emission time constant of trap, activation energy (E_a) is ($E_C - E_T$), σ_n is the capture cross section, and γ is a constant related to the effective electron mass. Additionally, a similar level, denoted as $E_C - 0.46$ eV with σ_n of $1.1 \times 10^{-14} \text{ cm}^2$, was observed in Czochralski-grown unintentionally doped (CZ UID) bulk Ga_2O_3 with the asymmetrically broadened DLTS signal.⁴³ In the literature, the energy depth of E1 also is similar to the $E_C - 0.4$ eV with σ_n of $1.5 \times 10^{-14} \text{ cm}^2$ calculated by the Arrhenius relationship in metal organic chemical vapor deposition (MOCVD)-grown Si-doped $\beta\text{-Ga}_2\text{O}_3$, which is possibly associated with point defects in $\beta\text{-Ga}_2\text{O}_3$.^{44,45} Hence, it is suggested that E1 may originate from the point defect located in the Ga_2O_3 layer. Emission time constant and capture time constant (τ_c) of trap can be extracted, as given by

$$\tau_e = \frac{1}{e_n} = \frac{1}{\gamma \sigma_n T^2} \exp\left(\frac{E_C - E_T}{kT}\right), \quad (5a)$$

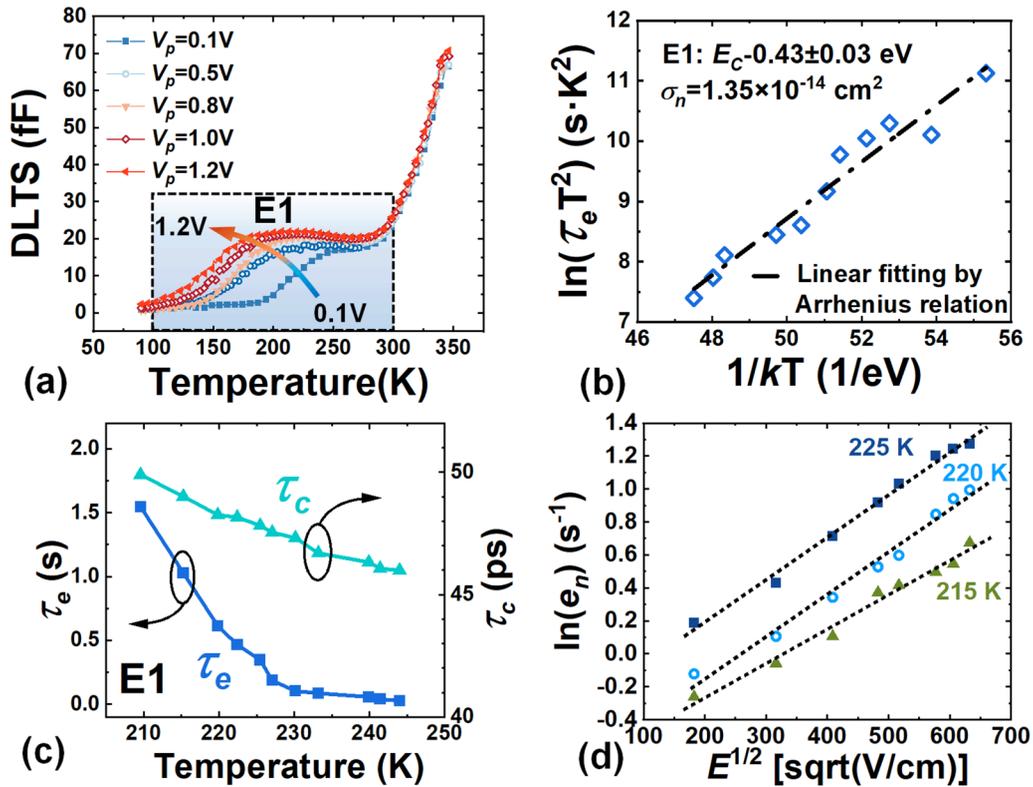


FIG. 4. (a) DLTS from 70 to 350 K with different pulse biases (V_p). (b) Arrhenius plot of discrete-level E1. (c) Temperature-dependent emission time constant (τ_e) and capture time constant (τ_c) of E1. (d) Electrical-field-dependent emission time of E1.

$$\tau_c = \frac{1}{v_{th,n} \sigma_n n_0}, \quad (5b)$$

where e_n is the reciprocal of τ_e , n_0 is the concentration of free electrons at the insulator/Ga₂O₃ interface, and $v_{th,n}$ is the thermal velocity of an electron. Both τ_e and τ_c show a decreasing trend with the increase of temperature as shown in Fig. 4(c). The extracted temperature-dependent τ_e of E1 was decreased from 1.55 s at 209 K to 27.4 ms at 244 K, indicating that the process of trapped electrons emitting from bulk trap E1 is thermal-accelerated. Assuming that the σ_n of E1 exhibits negligible temperature dependence within a narrow temperature range, the capture time constants of E1 show a slight decrease from 49.8 ps at 209 K to 45.9 ps at 244 K with increasing temperature. This observation suggests that the trapping process of E1 is significantly faster than its corresponding detrapping process.

Figure 4(d) illustrates the field dependence of the electron emission rate (e_n) of bulk trap E1 at temperatures, as indicated by DLTS spectra. The electron emission rate of E1 was determined for each fixed temperature ranging from 215 to 225 K. It is also observed that the carrier emission rates are significantly enhanced with an increased electric field at each temperature. Furthermore, the carrier emission mechanism can be modeled as trap-assisted Poole-Frenkel

emission (PFE) by plotting the logarithm of the emission rate $\ln(e_n)$ against the square root of the electric field ($E^{1/2}$).^{43,46} In the case of the defect state with Coulomb or similar potentials for thermal emission, the existence of a robust E -field within the depletion region leads to a reduction in the apparent thermal activation energy via the PFE mechanism.

Figure 5(a) presents the results of the isothermal capacitance transient spectroscopy (ICTS) measurement by varying T_m ,^{3,47} which was performed from 320 to 350 K to identify possible deeper bulk traps. The contour map of the temperature-dependent emission time distribution with the spectral amplitude of level E2 was also plotted. The primary signal peak denoting bulk trap E2 exhibits its smaller emission time constants with increasing temperature. In Fig. 5(b), τ_e of E2 was extracted from the main peaks of the ICTS signal, which was found to decrease from 5.57 to 0.47 s with increasing temperature from 320 to 350 K. The trapping process of E2 was slightly accelerated from 320 to 350 K, with τ_c decreasing marginally from 793 to 758 ps.

In Fig. 5(c), the Arrhenius plot was constructed for E2 to determine its activation energy level. The activation energy level of E2 was found to be 0.74 eV with a capture cross section of $6.60 \times 10^{-16} \text{ cm}^2$. It should be noted that the emission and capture time constants of E2 are both smaller than E1 together with relative

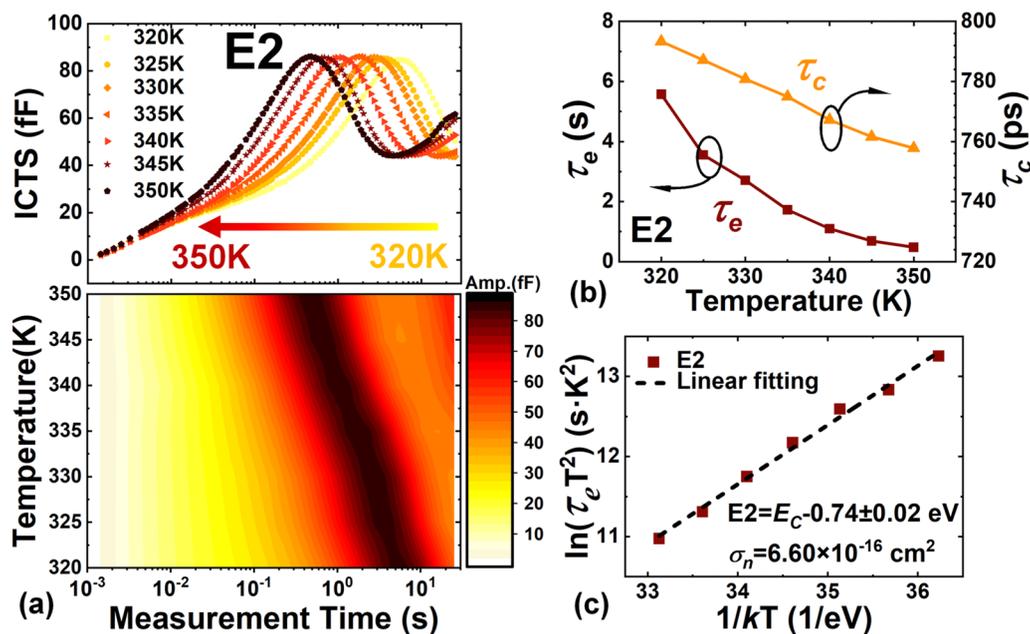


FIG. 5. (a) From 320 to 350 K, (top) ICTS varying T_m with fixed V_p of 1 V, V_m of -8 V, t_p of 100 ms along with (bottom) contour map of the emission time constant distribution. (b) Temperature-dependent emission time constant (τ_e) and capture time constant (τ_c) of E2. (c) Arrhenius plot of E2 extracted by ICTS.

larger activation energy of E2. This bulk trap E2 is similar to the previously revealed deep-state at $E_a = 0.71$ – 0.75 eV with σ_n of $(1.1$ – $17) \times 10^{-16}$ cm² in the Ga₂O₃ MOSFET.^{48,49} In the literature, one of the origins for the trap levels at $E_C - 0.73$ eV with σ_n of 1×10^{-14} cm² was attributed to the extrinsic defect iron impurity, such as Fe_{Ga}.^{50,51} However, in this study, due to the absence of iron impurities,^{52,53} the origin of E2 is likely attributed to an intrinsic source, perhaps from Ga vacancies or related complexes in Ga₂O₃.^{49,54} These facts about relaxation kinetics of E2 also can account for the drain current lag phenomenon and I_d – V_g hysteresis induced by the trap state at 0.75 eV in SiO₂/Ga₂O₃ MOSFETs, as reported in a previous study.⁴⁹

IV. CONCLUSIONS

In summary, a comprehensive analysis of the relaxation kinetic of interface states and bulk traps in a ZrO₂/β-Ga₂O₃ MOS capacitor was conducted in terms of bias and temperature dependence. The investigation of the energy distribution of trap states reveals the inclusion of continuum interface states and two bulk traps with discrete energy levels within Ga₂O₃. The analysis of trapping/detrapping relaxation kinetics for trap states in MOSCAPs has been conducted in the time-domain by altering the gate bias, revealing a stretched-exponential transient decay. The distribution of interface states was obtained over a wide range of 0.1–0.7 eV below the conduction band edge. From 3D mapping of capacitance transient, at higher positive pulse bias, both the interface state density and the population of trapped charges become increased.

The thermally stimulated capture and emission behavior of interface states were quantitatively analyzed.

Two bulk traps E1 and E2 were identified with the discrete activation energies of 0.43 and 0.74 eV, respectively. With increasing temperature, the emission process of bulk traps is accelerated, while the trapping process exhibits minimal sensitivity to temperature changes. The detrapping process of carriers by E1 can be promoted by an electric field and can be modeled as Poole–Frenkel emission. An anomalous C–V hysteresis is observed, which varied the applied gate bias. In a bidirectional C–V sweep, after upward sweeping with a fast charging process, the carrier detrapping with a longer emission time constant of trap states leads to a pronounced C–V hysteresis instability.

These results pertaining to properties of interface states and bulk traps hold significant implications for minimizing the trap density, improving the interfacial properties and optimizing fabrication processes, thereby enhancing the stability and performance of Ga₂O₃ MOSFETs.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jiaxiang Chen: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (lead); Methodology (lead); Validation (equal); Writing – original draft (lead); Writing – review & editing (equal). **Haolan Qu:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Visualization (equal). **Jin Sui:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (supporting); Validation (equal); Visualization (equal). **Xing Lu:** Conceptualization (equal); Methodology (equal); Resources (supporting). **Xinbo Zou:** Conceptualization (equal); Funding acquisition (equal); Methodology (equal); Project administration (lead); Resources (equal); Supervision (lead); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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