Temperature-Dependent Dynamic Degradation of Carbon-Doped GaN HEMTs

Yitian Gu, Yangqian Wang, Jiaxiang Chen, Baile Chen, *Member, IEEE*, Maojun Wang, *Member, IEEE*, and Xinbo Zou, *Member, IEEE*

***Abstract*— Temperature-dependent dynamic degradation was investigated for C-doped GaN high electron mobility transistor (HEMT) from 300 to 20 K. Pulsed *I–V* measurements with various OFF-state quiescent bias voltages revealed that current collapse (C.C.) induced by charge-trapping effect at room temperature was greatly suppressed and monotonously declined as decreasing temperatures. This was attributed to reduced number of electrons which were injected into the C-doped layer and capable of overcoming capture potential barrier. Drain current transient measurements were employed to investigate temperature-dependent and time-resolved carrier capture/emission process. Based on the extracted time constants, an activation energy of 0.36 eV was identified for the electron capture process. For carrier emission process, both current-based and capacitance-based transient analysis indicated an activation energy around 0.20 eV. Furthermore, the traps were confirmed to be located in the C-doped layer by varying the pulse stimulus in deep-level transient spectroscope (DLTS). The measurement results showed that C-doped HEMTs grown on Si substrates exhibited high-saturation current, stabilized threshold voltage, and minor C.C. at cryogenic temperatures, particularly in comparison with those at room temperature.**

***Index Terms*— Carbon-doped GaN, cryogenic temperatures, dynamic characteristics, GaN high electron mobility transistor (HEMT), low-temperature electronics.**

I. Introduction

AlGaN/GaN-BASED high electron mobility transistors (HEMTs) have garnered considerable research interests due to superior material properties and device characteristics, including high carrier mobility, substantial conduction current density, and large breakdown voltage [1]–[3].

In the last decades, extensive efforts have been put into the improvement of GaN-based HEMTs [4]–[6]. Carbon (C) doping has been proposed and introduced in the GaN buffer to avoid bulk leakage and current punchthrough along the buffer [7]. However, C-dopants may generate deep-level states within the bandgap of GaN and result in current dispersions [8]–[11]. Current collapse (C.C.) and buffer leakage current were identified to be associated with carbon-doping level. The HEMT with carbon-doping concentration of 8×10^{17} cm^{-3} exhibited C.C. over 35% and buffer leakage current close to 0.1 μA/mm $\cdot$ at 200 V. To suppress the current dispersions in the C-doped HEMTs, a stepped carbon-doping scheme was reported to tune the carbon dopant distribution as well as the way carbon was incorporated [12], [13]. Apart from optimized C-doping scheme, mitigated C.C. in C-doped HEMT has been reported by passivation layers, field plates, and an alternative Fe-doped buffer [14]–[16].

One of our recent studies on an unpassivated HEMT suggested that a low temperature of 150 K may help achieve much stabilized threshold voltage and mitigated C.C. [17], in addition to improved HEMT dc performance at cryogenic temperatures, which has been widely reported in the literature [18]–[21]. Despite the fact that a comprehensive comparative study at two temperature steps has been carried out [17], however, there are still several relevant issues to be addressed.

1) In the case of AlGaN/GaN HEMT with a C-doped buffer, what would the dynamic performance be at cryogenic temperatures under 77 K? Is there a temperature dependence for the C.C. below room temperature?
2) Previous dynamic study on an unpassivated HEMT at 150 K suggested existence of a capture potential barrier which would hinder electron trapping, particularly at a low temperature. However, a quantitative assessment of the activation energy for electron capture process is still missing.
3) In addition to the extent of C.C., a time-resolved recovery process at various temperatures is still unclear, which obstructed a deeper understanding of trap emission process for C-doped HEMTs.

In this study, temperature-dependent dynamic characteristics of C-doped GaN HEMTs were analyzed.

Manuscript received February 13, 2021; revised April 11, 2021; accepted April 28, 2021. This work was supported in part by the ShanghaiTech University Startup Fund and sponsored by Shanghai Pujiang under Program 18PJ1408200, in part by the Shanghai Eastern Scholar (Youth) Program, and in part by the Chinese Academy of Sciences (CAS) Strategic Science and Technology Program under Grant XDA18000000. The review of this article was arranged by Editor K. Alam. *(Yitian Gu and Yangqian Wang contributed equally to this work.) (Corresponding authors: Xinbo Zou; Maojun Wang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3077345.

Digital Object Identifier 10.1109/TED.2021.3077345

1) C.C. was quantitatively investigated from 300 to 20 K, by means of various OFF-state quiescent bias voltages and drain-gate-delay (DGD) durations.
2) Based on "fast sweeping" I–V measurements, given a fixed gate stress ($V_{gs} = -10$ V), V_{th} instability induced by electron trapping/detrapping was analyzed employing various stress/recovery durations.
3) Drain current transient measurements were utilized to quantitatively assess the capture/emission time constant. Activation energy for the electron capture/emission process was extracted from Arrhenius plots as well.

II. Experiment

The HEMT device (provided by NTT-AT) used in this article, was grown on a 6-in Si substrate by metal organic chemical vapor deposition (MOCVD) and consisted of 4-μm-thick C-doped buffer layer, a 300-nm undoped GaN layer, and a 30-nm undoped $Al_{0.25}Ga_{0.75}N$ barrier layer as shown in Fig. 1(a). The device used Ti/Al/Ni/Au (20 nm/160 nm/50 nm/100 nm) as ohmic contact after mesa isolation. A 150-nm-thick Si_3N_4 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C and then annealed for 10 min in N_2 at 400 °C. Then reactive-ion etching (RIE) gate-opening was implemented for Ni/Au gate metal deposition and interconnection.

The gate width/length of the device in this study was 20 μm/1.5 μm ($W_g = 20$ μm and $L_g = 1.5$ μm). The distances from gate–drain and to source were 3 and 2 μm, respectively ($L_{gd} = 3$ μm and $L_{gs} = 2$ μm). Pulsed I–V and "fast sweeping" I–V measurements were performed on the GaN HEMT from 300 to 20 K. These measurements employed Keysight Waveform Generator/Fast Measurement Unit (WGFMU) B1530A and B1500A semiconductor device parameter analyzer for data acquisition. In the pulsed I–V measurements, the pulsewidth was set as 10 μs to measure the dynamic performances of GaN HEMTs at different quiescent OFF-state bias voltages. For "fast sweeping" I–V measurements, a fixed negative gate bias was applied on the sample for various stress/recovery durations, followed by measurement steps, each of which consisted of 250 ns rise time and 250 ns measurement time. The total sweeping measurement process was completed within 50 μs. Drain current transient and deep-level transient spectroscopes (DLTS) were also utilized to assess the trap-related information.

III. Results and Discussion

Fig. 1(b) and (c) showed the transfer (plot in semilog and linear scale) and transconductance characteristics of C-doped GaN HEMT grown on Si from 300 to 60 K without any pre-stressing conditions. Using the 1 mA/mm standard, the threshold voltage (V_{th}) was hardly shifted ($V_{th} = -5.20$ V with a standard deviation of 0.06 V) and the subthreshold slope (SS) was reduced from 142.6 to 89.7 mV/dec as the environment was cooled down to 60 K. In addition, the drain current density achieved its maximum value at 100 K, where it was more than twice of that at 300 K. At $V_{gs} = -2$ V and $V_{ds} = 1$ V, the drain current was increased from 124 mA/mm (300 K) to

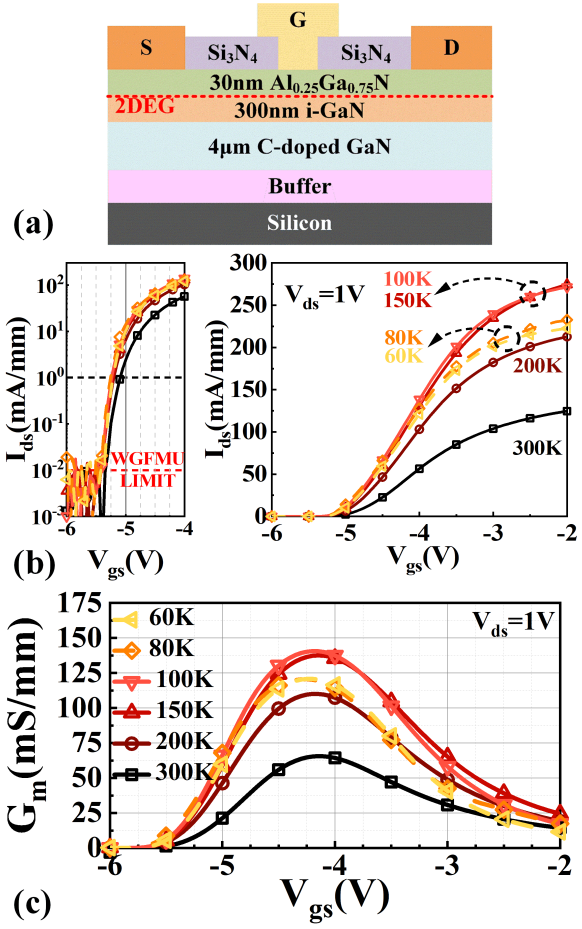

Fig. 1. (a) Schematic cross section of C-doped GaN HEMT grown and fabricated on silicon. (b) Transfer characteristics (plot in semilog and linear scale). (c) Transconductance characteristics of GaN HEMT from 300 to 60 K.

TABLE I
Temperature-Dependent Field-Effect Mobility

T(K)	300	200	150	100	80	60	20
μ(cm²/Vs)	1025	1288	1532	1606	1460	1448	1461

271 mA/mm (100 K). The improvement of device performance was due to the reduction of thermal lattice vibration scattering at low temperatures, which enhanced the electron mobility in the two-dimensional electron gas (2DEG) channel [22].

The temperature-dependent field-effect carrier mobility has been extracted [23] and summarized in Table I, in which electron mobility achieved its maximum value at 100 K (1606 cm²/Vs), in a good agreement with temperature-dependent electron mobility reported in [24].

Correspondingly, the GaN HEMT exhibited much better transconductance characteristics at cryogenic temperatures, according to

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = C_g \frac{W}{L} \mu V_{DS} \quad (1)$$

where C_g is the gate capacitance per unit area. The transconductance was increased to 141 mS/mm at 100 K due to

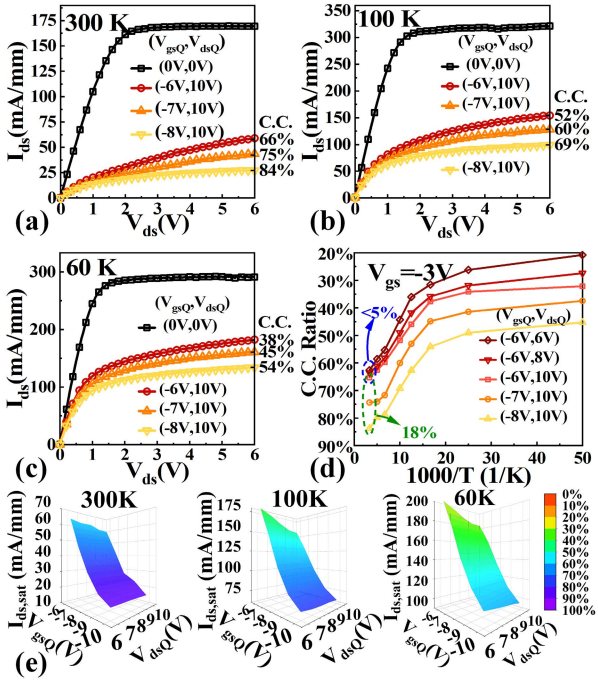

Fig. 2. (a)–(c) Pulsed I_{ds}–V_{ds} characteristics of GaN-based HEMTs with various quiescent voltages at 300, 100, and 60 K. (d) Extracted C.C. ratio as a function of temperature and quiescent bias. (e) 3-D mapping of GaN HEMT C.C. under different stress conditions at 300, 100, and 60 K.

enhanced carrier mobility in 2DEG channel. At an even lower temperature under 100 K, the transconductance slightly dropped to 120 mS/mm due to marginally decreased mobility, probably by deformation potential or piezoelectric scattering [25].

Pulsed I–V measurements were employed to reveal the dynamic characteristics of C-doped GaN HEMT. It consisted of three phases: (1) stressing at various quiescent bias voltages: V_{gsQ} below V_{th} along with drain bias V_{dsQ} was applied for 2 ms to guarantee sufficient electron injection, (2) switching phase: V_{gs} was increased to be above V_{th} with V_{ds} dropped to a lower bias level, and 3) operation phase: V_{gs} was kept above V_{th} and drain bias was set as various values to measure the output characteristics.

Fig. 2(a) displayed the pulsed I_{ds}–V_{ds} (measured at $V_{gs} = -3$ V) with various quiescent voltage combinations at 300 K. The current dispersion phenomenon was highly dependent on gate stressing conditions. The C.C., which was defined as $(1 - I_{sat,stress}/I_{sat,fresh}) \times 100\%$, was calculated to be 66% with $V_{gsQ} = -6$ V. With V_{gsQ} being strengthened from -6 to -8 V, the C.C. was further increased to 84%. This phenomenon can be explained by electron injection due to V_{gsQ} as well as high lateral electrical field [26]. When the C-doped GaN HEMTs suffered from OFF-state quiescent bias ($V_{gsQ} < V_{th}$, $V_{dsQ} = 10$ V), electrons injected from the gate entered the continuum electronic states of C-doped layer and then overcame a capture potential barrier, and got captured by a trap state [17]. Once the device was switched to ON-state, electrons being trapped in the traps of C-doped buffer cannot be released instantaneously, and the 2DEG in channel would remain partially depleted [1], leading to C.C. and increased dynamic resistance. While at 100 and 60 K, as shown in

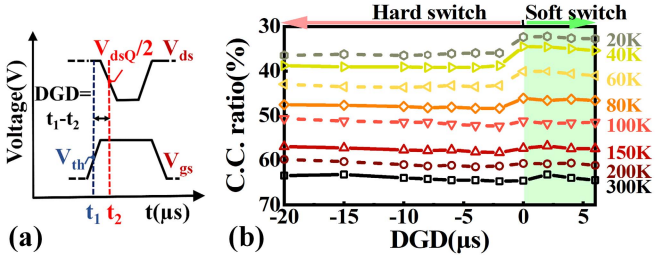

Fig. 3. (a) Pictorial illustration of DGD which was defined as the time difference between a drain voltage reducing to $V_{dsQ}/2$ and V_{gsQ} reaching V_{th}. (b) C.C. ratio as a function of DGD and temperature ($V_{gsQ} = -6$ V and $V_{dsQ} = 10$ V).

Fig. 2(b) and (c), the C.C. was much alleviated using the same quiescent bias at cryogenic temperatures. For example, given V_{gsQ} of -8 V and V_{dsQ} of 10 V, alleviated C.C. of 69% and 54% were observed for 100 and 60 K, respectively. This was attributed to two factors. One is the number of electrons injected into the C-doped layer from the gate was much reduced at cryogenic temperatures. The other one is the decreased population of electrons overcoming the energy potential barrier due to limited thermal energy [17].

Specifically, C.C. phenomena as a function of V_{gsQ} and V_{dsQ} were mapped from room temperature to cryogenic temperatures, as shown in Fig. 2(d) and (e). At 300 K, the change of V_{dsQ} from 6 to 10 V has a minor impact on worsening C.C. (<5%). Enlarging V_{gsQ} from -6 to -8 V has been experimentally identified as the key factor leading to extra C.C. (∼18%). One may find for each temperature step, V_{gsQ} played a dominant role in determining C.C. compared with V_{dsQ}, probably due to the surface passivation in the access region. Furthermore, C.C. was alleviated significantly as the temperature was decreased, in addition to much improved conduction current density. C.C. effect commonly observed at 300 K was well suppressed at cryogenic temperatures, suggesting inefficient charge-trapping effects at cryogenic temperatures or a capture barrier needed to be overcome before electrons got trapped [27].

In addition to soft switch conditions, the device was also measured at hard switch conditions for further studying hot electron effect at low temperatures. Hard switch or soft switch could be tuned by setting DGD time [Fig. 3(a)] as a positive or negative value, where DGD was defined as the time difference between a drain voltage reducing to $V_{dsQ}/2$ and V_{gsQ} reaching V_{th}. Fig. 3(b) depicted the C.C. ratio when the device was tested at $V_{gsQ} = -6$ V and $V_{dsQ} = 10$ V, using various DGD durations. Compared with the soft-switching case, additional C.C. was only observed under 100 K using a hard-switching mode, despite the fact that the average kinetic energy of carriers in the channel was pushed to the equipment limit (V_{dsQ} of 10 V). For example, the C.C. was only slightly increased from 32% (soft switch) to 36% (hard switch) at 20 K. Thus, hot electrons did not promote remarkable extra trapping process nor generate new trap states in this passivated C-doped HEMT on Si with the above measurement parameters.

To quantitatively assess the charge trapping effect in the pulsed measurements, the V_{th} instability was monitored by "fast-sweeping" I–V measurements after various stress dura-

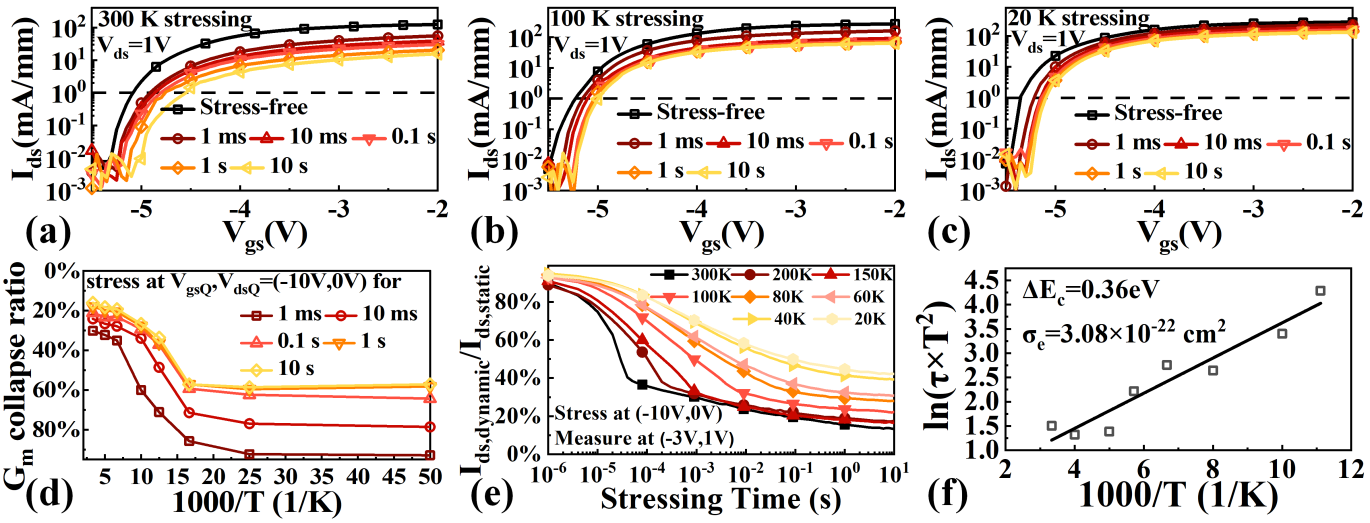

Fig. 4. (a)–(c) Threshold voltage instability measurement results with various reverse gate bias stressing durations ($V_{gs} = -10$ V) at 300, 100, and 20 K. (d) Extracted peak transconductance collapse ratio as a function of temperature and stressing duration. (e) Drain current ratio as a function of temperature and OFF-state periods. (f) Arrhenius plot for the trapping process based on current transient measurements.

tions (1, 10 ms, 0.1, 1, and 10 s). In these measurements, only the gate terminal was reverse biased and drain terminal was grounded with source ($V_{gs} = -10$ V and $V_{ds} = 0$ V) due to its minor influence according to the experiment results in Fig. 2. Fig. 4(a)–(c) showed the transfer characteristics as a function of stressing durations at 300, 100, and 20 K, respectively. Using the 1 mA/mm standard, the threshold voltage (V_{th}) was shifted positively: $\Delta V_{th} = 0.17$ V after 1 ms stressing and ΔV_{th} reached 0.53 V after 10 s stressing, along with degradation of transconductance at 300 K. The positive V_{th} shift and decrease in the transconductance were originated from traps in C-doped layer, close to the gate terminal. When a high reverse gate bias was applied, electrons were injected into C-doped buffer and trapped. At 100 and 20 K, the V_{th} shift was limited to 0.18 and 0.11 V, respectively, after stressing for 10 s. In addition, the transconductance collapse ratio, which was defined as $(1 - G_{m,stress}/G_{m,fresh}) \times 100\%$, was extracted and shown in Fig. 4(d). The ratio was highly dependent on temperatures and OFF-state stressing durations. For example, the degradation of transconductance was suppressed from 84% to 43% as the temperature decreased from 300 to 20 K after stressing duration of 10 s.

To further study the time-resolved behaviors of traps, drain current transient measurements were performed. The drain current was measured at a fixed voltage combination ($V_{gs} = -3$ V and $V_{ds} = 1$ V) after various stressing periods. Fig. 4(e) plotted C.C. as the function of stressing duration and temperature. At 300 K, the ratio was suppressed from 89% to 13% after the device subjecting to stressing time from 1 μs to 10 s. The dynamic current ratio was improved as the environment was cooled down. At 20 K, the ratio was improved to 93% at 1 μs and 42% at 10 s. The current ratio could be well described by a stretched exponential function of the form

$$\frac{I_{ds,dynamic}}{I_{ds,static}}(t) = \frac{I_{final}}{I_{ds,static}} + A\exp\left(-\frac{t}{\tau_c}\right) \quad (2)$$

where t is the OFF-state stress time, τ_c is the capture time constant of electron traps, and A is a constant related to I_{final}. The capture time constant could be identified and extracted from Fig. 4(e) by locating the peak of $\partial I_{ds}/\partial \log_{10}(t)$. Upon gaining the capture time constant, one may use the following Arrhenius law [28] to extract σ_e, the emission cross section and ΔE_c, the activation energy for the electron capture process

$$\ln\left(\frac{T^2}{e_c}\right) = \frac{\Delta E_C}{k_B T} - \ln(\sigma_e \gamma_n) \quad (3)$$

where $e_c = 1/\tau_c$ and γ_n is the constant related with the effective mass of carrier ($\gamma_n = (4\sqrt{6}\pi^{3/2} m_n^*/h^3)$).

At 300 K, capture time constant was extracted to be 50 μs and at 100 K, the capture time constant was prolonged to be 3 ms. For temperatures below 100 K, the capture time constant was typically pinned around 10 ms. The Arrhenius plot revealed an activation energy of 0.36 eV (ΔE_c) and emission cross section (σ_e) of 3.08×10^{-22} cm^2 for the electron capture process. The alleviated dynamic characteristic degradation at cryogenic temperatures was attributed to the inefficient charge-trapping as a result of the existence of a capture potential barrier and limited thermal energy.

Recovery process upon applications of reverse bias stressing was also examined. For each temperature step, after OFF-state stressing at $V_{gs} = -10$ V and $V_{ds} = 0$ V, the V_{th} was approaching to its stress-free value gradually as the "recovery time" was extended from 1 ms to 10 s. A typical evolution of the recovery process is shown in Fig. 5(a), which illustrated gradual shift of transfer curves for the C-doped HEMT on Si at 100 K. As the electrons trapped in C-doped buffer were released and emitted during recovery process, a negative shift of V_{th} was observed.

In order to understand the temperature dependent emission process, drain current transient recovery measurements were carried out for C-doped HEMTs. During the OFF-state stressing, the device was biased at $V_{gs} = -10$ V and $V_{ds} = 0$ V. Then, current was measured by pulsed voltage stimulus

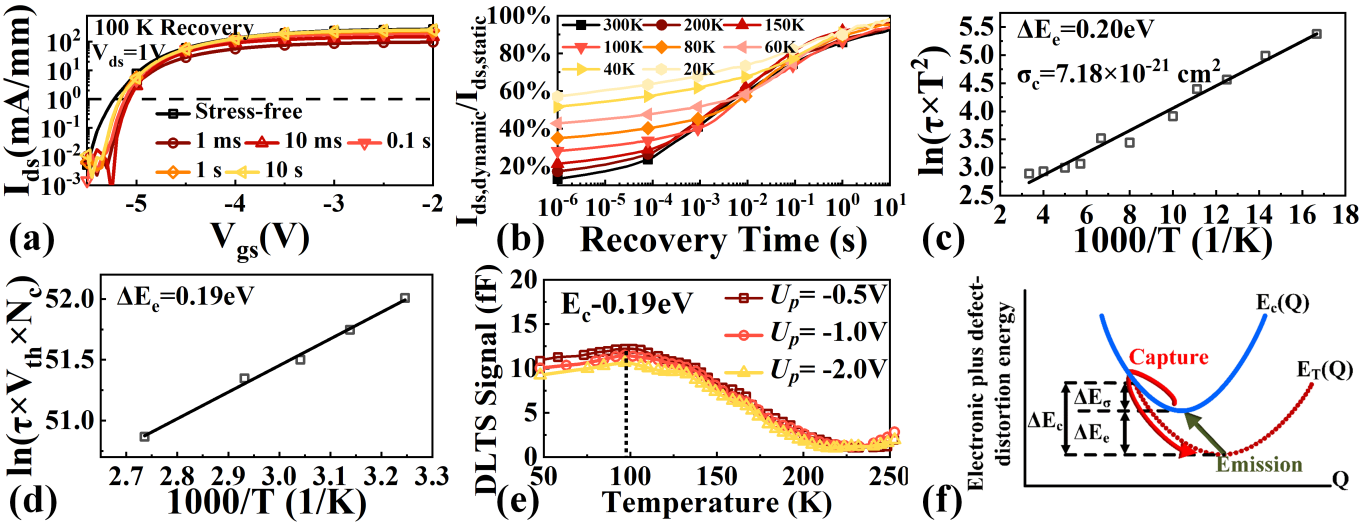

Fig. 5. (a) Threshold voltage instability measurement results with various recovery durations (V_{gs} = 0 V and V_{ds} = 0 V) after gate bias stress (V_{gs} = −10 V, 10 s) at 100 K. (b) Drain current ratio as a function of temperature and recovery period. (c) and (d) Arrhenius plot for carrier emission process based on the current and capacitance transient measurements. (e) DLTS spectra of the C-doped GaN SBD with U_p varying from −0.5 to −2.0 V. (f) Configuration coordinate diagrams for trap state [$E_T(Q)$] and the conduction band [$E_c(Q)$]. Free electrons should overcome the additional energy heights (ΔE_σ) to be trapped. ΔE_c and ΔE_e are the activation energy for the electron capture process and electron emission process, respectively.

(V_{gs} = −3 V and V_{ds} = 1 V). Fig. 5(b) reported transient features of dynamic current ratio from 300 to 20 K as a result of the carrier detrapping process. The drain current dynamic/static ratio was resumed from 12% to 92% at 300 K after 10 s recovery time. However, at 20 K, the recovery of current ratio began with a number of 57% due to alleviated capture process. After 10-s recovery, the drain dynamic current was recovered to 97% of its static value. The time-dependent current ratio could be well described by

$$\frac{I_{\mathrm{ds,dynamic}}}{I_{\mathrm{ds,static}}}(t) = \frac{I_{\mathrm{final}}}{I_{\mathrm{ds,static}}} - A\exp\left(-\frac{t}{\tau_e}\right) \tag{4}$$

where t is the recovery duration, τ_e is the emission time constant of electron traps, and A is a constant related to I_{final}. The emission time constant could be identified and extracted from Fig. 5(b) by locating the peak of $\partial I_{ds}/\partial \log_{10}(t)$. Upon obtaining emission time constant, the capture cross section σ_c and ΔE_e, the activation energy for the electron emission process could be extracted

$$\ln\left(\frac{T^2}{e_e}\right) = \frac{\Delta E_e}{k_B T} - \ln(\sigma_c \gamma_n) \tag{5}$$

where $e_e = 1/\tau_e$ and γ_n is the constant related with the effective mass of carrier ($\gamma_n = (4\sqrt{6}\pi^{3/2} m_n^*/h^3)$).

The extracted emission time constant was elongated from 200 μs to 60 ms as the temperature was decreased from 300 to 60 K, and barely changed for even lower temperatures. An Arrhenius plot of the emission process [Fig. 5(c)] showed that an activation energy of 0.20 eV (ΔE_e) with a capture cross section (σ_c) of 7.18 × 10^{-21} cm^2 was extracted for the electron emission process. Meanwhile, a capacitance-based DLTS (C-DLTS) measurement on a Schottky barrier diode (SBD) revealed that an activation energy of 0.19 eV was extracted for the electron emission process [Fig. 5(d)], in line with the results by the current transient method. The extracted capture and emission process parameters [29] are illustrated in Fig. 5(f). Free electrons need to overcome additional energy heights (ΔE_σ) to be trapped at the trap level [30]. The activation energy for the electron capture process (ΔE_c) and the activation energy for the electron emission process (ΔE_e) are also illustrated in the graph.

In order to determine the location of the traps, DLTS with various filling pulse levels was employed. Fig. 5(e) recorded the DLTS signal results with the fixed reverse bias (U_R = −5 V) and various filling pulse voltages (U_p = −0.5 V, −1.0 V, or −2.0 V). The peak amplitudes of the multiple measurements were typically unchanged with varying U_p. The results suggested uniformly distributed trap which did not exert influence on the trap emission rate and indicated that the trap states are located in the C-doped GaN layer, rather than the device surface [31]. In addition, the trap level revealed by either capacitance or current transient method matched well with reports about GaN based devices with carbon doping [32].

IV. Conclusion

DC and dynamic characteristics as a function of temperature were investigated for C-doped GaN HEMTs on Si, from room temperature to cryogenic temperatures. Saturation current density and transconductance were found to be increased from 300 to 100 K as a result of enhanced carrier mobility. C.C. induced by charge-trapping effect at room temperature was greatly suppressed and monotonously declined as decreasing temperatures. Stabilized V_{th} and diminished transconductance degradation were observed for cryogenic temperatures. This was attributed to reduced number of electrons which were injected into the C-doped layer and capable of overcoming capture potential barrier. For each temperature step, V_{gsQ} played a dominant role in determining C.C. compared with V_{dsQ}, due to surface passivation in the access region. Drain current transient measurements help quantitatively assess the capture/emission time constant. The capture time constant

was prolonged from 50 μs (300 K) to 10 ms (20 K) as the temperature was decreased. This phenomenon provided the experimental evidence to suppress trapping behaviors at low temperatures. The emission time constant was also extended from 200 μs (300 K) to 60 ms (20 K). In addition, activation energy of 0.36 and 0.20 eV were extracted for the electron capture process and emission process, respectively. Capacitance-mode DLTS on a SBD revealed a similar activation energy for the electron emission process (ΔE_e = 0.19 eV), in a good agreement with the current transient emission results. Furthermore, the traps were confirmed to be located in the C-doped layer by varying the pulse stimulus levels in the DLTS measurements.

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