Temperature-Dependent Dynamic Performance of p-GaN Gate HEMT on Si

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***Abstract*— Temperature-dependent dc and dynamic characteristics of p-GaN gate HEMT were thoroughly investigated from 300 to 140 K. At low temperature, in addition to barely shifted threshold voltage, substantial improvement in drain current was observed. At 300 K both positive and negative gate bias stressing were applied to the device in order to form a complete mapping of threshold voltage instability of p-GaN gate HEMT. Three mechanisms, namely hole trap emission, carrier out-spilling, and hole accumulation have been employed to elucidate the trends of threshold voltage shift at room temperature. Temperature-dependent dynamic performances, including threshold voltage instability and drain current degradation, were investigated. Via drain current transient spectroscopy, activation energy for hole emission and trapping process were extracted as 132 and 70 meV, respectively. Detailed pulsed output characteristics at various quiescent biases were explored. At 300 K, gate quiescent bias played a dominant role in determining current collapse compared with drain quiescent bias. Moreover, current collapse caused by gate pulse stressing was much mitigated with decrease of temperature. The detailed temperature-reliant dynamic performance provides valuable information for justifying feasibility of p-GaN gate HEMT for low-temperature applications and further device optimizations.**

Manuscript received December 7, 2021; revised January 17, 2022 and March 31, 2022; accepted April 8, 2022. Date of publication April 26, 2022; date of current version May 24, 2022. This work was supported in part by ShanghaiTech University Startup Fund under Grant 2017F0203-000-14, in part by the National Natural Science Foundation of China under Grant 52131303, in part by the Natural Science Foundation of Shanghai under Grant 22ZR1442300, and in part by CAS Strategic Science and Technology Program under Grant XDA18000000. The review of this article was arranged by Editor S. Choi. *(Yitian Gu and Wei Huang contribute equally to this work.) (Corresponding authors: Wei Huang; Xinbo Zou.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3167342.

Digital Object Identifier 10.1109/TED.2022.3167342

***Index Terms*— Dynamic characteristics, GaN HEMT, low temperature electronics, p-type GaN gate.**

I. Introduction

AlGaN/GaN-BASED high electron mobility transistors (HEMTs) have been regarded as promising candidates for next-generation high-power high-frequency systems [1]–[3], due to outstanding III-N material properties, including wide bandgap, high electron saturation velocity, and large critical electrical-field. In recent years, normally off III-N transistors based on AlGaN/GaN heterostructure with high two-dimensional electron gas (2DEG) density have garnered considerable research attention to meet the fail-safe design requirement. Extensive efforts have been devoted into the fabrication of normally off GaN HEMT, aiming at depleting 2DEG under the gate while keeping 2DEG in the access region [4]. Gate recess [5], [6], ion implantation [7], [8], and p-GaN gate [9], [10] are three representative ways to achieve normally off operations. Normally off AlGaN/GaN HEMT by two-step gate recess was reported in Chang *et al.* [11], demonstrating threshold voltage of 0.68 V, maximum drain saturation current of 228.9 mA/mm and peak transconductance of 107.2 mS/mm. Fluorine-implanted AlN/GaN HEMTs fabricated lately could reach a threshold voltage of 0.35 V [12]. For p-GaN gate HEMT, adjustment of the threshold voltage via composite barrier design together with high saturation current has been reported [13], [14].

Recently dynamic performance of p-GaN gate HEMT, particularly its threshold voltage instability induced by positive gate bias and OFF-state drain stress, has been investigated and documented [15]–[20]. With positive gate bias, it is revealed that electron–hole recombination, electron trapping, and hole accumulation are three major mechanisms to explicate the threshold voltage shift [19]. Above room-temperature threshold voltage shift upon positive gate bias was also reported [20]. Accelerated recovery process was spotted as increasing the temperature. With OFF-state drain stressing, positive shift of threshold voltage was observed from both experimental measurements and TCAD simulations [21].

Though threshold voltage instability of p-GaN gate HEMT has been amply investigated, there are still several concerns to be addressed before reaching a comprehensive understanding of dynamic performance of p-GaN gate HEMT.

1) The temporal behavior of drain current during the stressing process and recovery process was unclear for p-GaN

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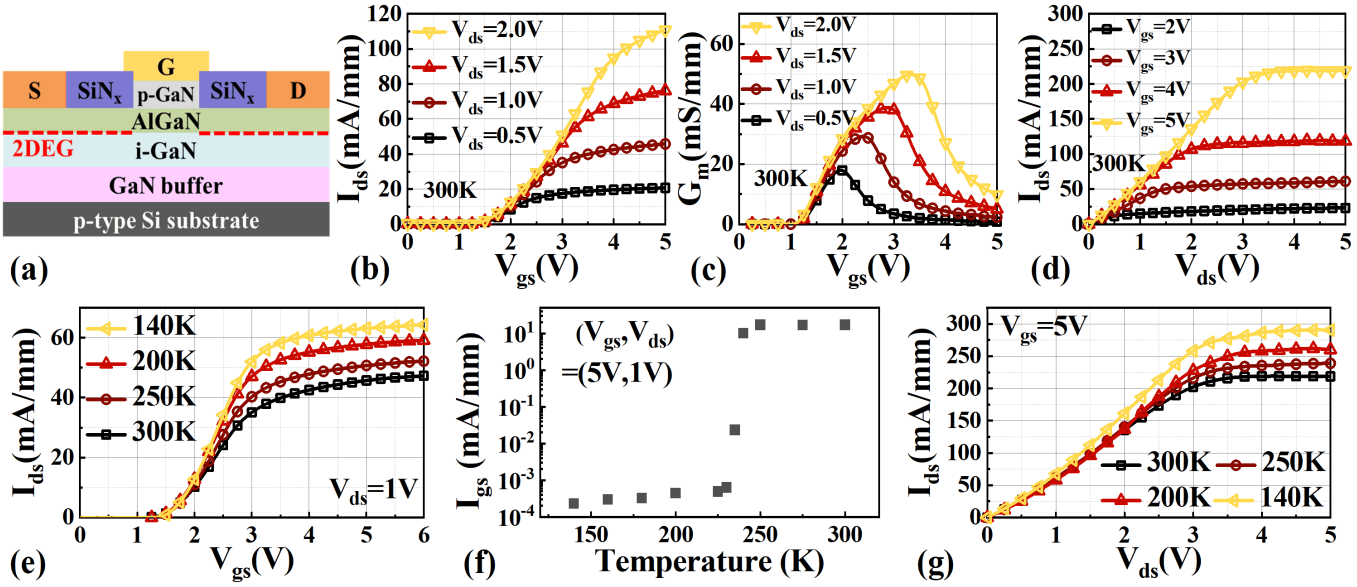

Fig. 1. (a) Schematic cross section of p-GaN gate HEMT. (b)–(d) Transfer characteristics, transconductance characteristics, and output characteristics of p-GaN gate HEMT at room temperature. (e) Transfer curves of p-GaN gate HEMT at $V_{ds} = 1$ V from 300 to 140 K. (f) Extracted ON-state gate current for $V_{gs} = 5$ V $V_{ds} = 1$ V. (g) Output curves of p-GaN gate HEMT at $V_{gs} = 5$ V from 300 to 140 K.

gate HEMT. In addition, most investigations of threshold voltage instability focus on effects of positive gate bias. There is still a lack of mapping for threshold voltage instability covering a wide range of gate biases from OFF- to ON-state.

2) Temperature-dependent dynamic performance, particularly those at temperatures below room temperature is absent, which hindered the use of p-GaN gate HEMT for low-temperature applications such as orbiting spacecraft or superconducting [22]. Additionally, activation energy associated with carrier capture/emission process for p-GaN gate HEMTs remain unknown.
3) Previous study for p-GaN gate HEMT mainly focused on the impact of drain voltages with grounded gate voltages [1], [23]. There is insufficient investigation on switching performance with negative gate quiescent bias, in the pulsed current collapse measurements. Little attention was paid to the comparison between impact of gate bias and drain bias.

In this study, dynamic performance of p-GaN gate HEMT was thoroughly investigated.

1) Threshold voltage instability with both positive and negative gate biases was measured and interpreted. The mapping of threshold voltage shift was divided into three stages, and the mechanism for each stage was revealed. In addition, time-resolved dynamic drain current at a fixed gate bias was studied.
2) Temperature-dependent drain current transient spectroscopy was performed from 300 to 140 K. With negative gate bias, time constant, and activation energy of relevant hole traps for both carrier emission process and capture process were fully revealed and extracted.
3) Detailed switching on measurements with various gate and drain quiescent biases combinations were addressed, to characterize the current collapse of the p-GaN gate HEMT in a wide temperature range. Impact of quiescent bias from the gate terminal and drain terminal was comparatively disclosed. Much alleviated current collapse with gate quiescent bias was observed as decreasing the temperature.

The explicit temperature-dependent dynamic performance provides valuable information to justify applicability of p-GaN gate HEMT for low-temperature applications and shed insight on further device optimizations.

II. Experiment

The p-GaN gate HEMT used in this study was grown by metal-organic chemical vapor deposition (MOCVD) and consisted of 3.5-μm-thick buffer layer, a 200 nm undoped GaN layer, and a 15 nm undoped $Al_{0.23}Ga_{0.77}N$ barrier layer. The top 75 nm p-GaN layer was grown with a Mg doping concentration of 3×10^{19} cm^{-3}, as shown in Fig. 1(a). Gate metal was deposited on the p-GaN layer to form a Schottky-type contact. The gate width/length of the device in this study was 100/3.5 μm ($W_g = 100$ μm, $L_g = 3.5$ μm). The distances from gate to drain and to source were 12 and 2.5 μm, respectively ($L_{gd} = 12$ μm, $L_{gs} = 2.5$ μm). The device was passivated by a SiN_x layer.

Details of the bias-induced threshold instability measurement can be found from our previous publication [24]. The whole measurement process was completed in 75 μs to maximize the retention of device transient state. Drain current transient spectroscopy was employed to show time-dependent stressing and recovery process. The device was stressed at various gate biases and recovered naturally. Pulsed measurements with various gate and drain quiescent bias combinations were performed by repeatedly switching the device ON and OFF, to monitor the current collapse.

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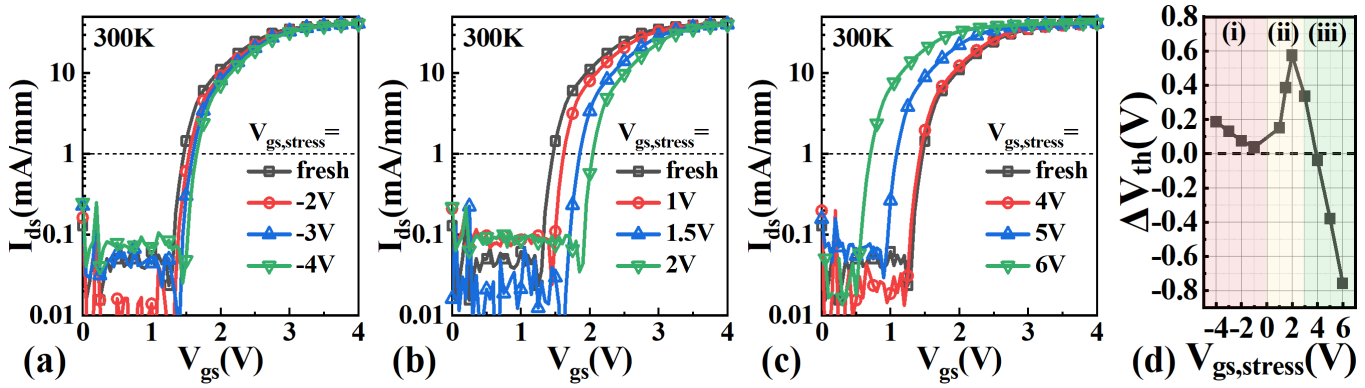

Fig. 2. (a)–(c) Gate bias induced threshold instability under various gate bias voltage from −4 to 6 V for 1 s at 300 K. The transfer curves were measured at V_{ds} = 1 V. (d) Extracted threshold voltage shift from (a)–(c).

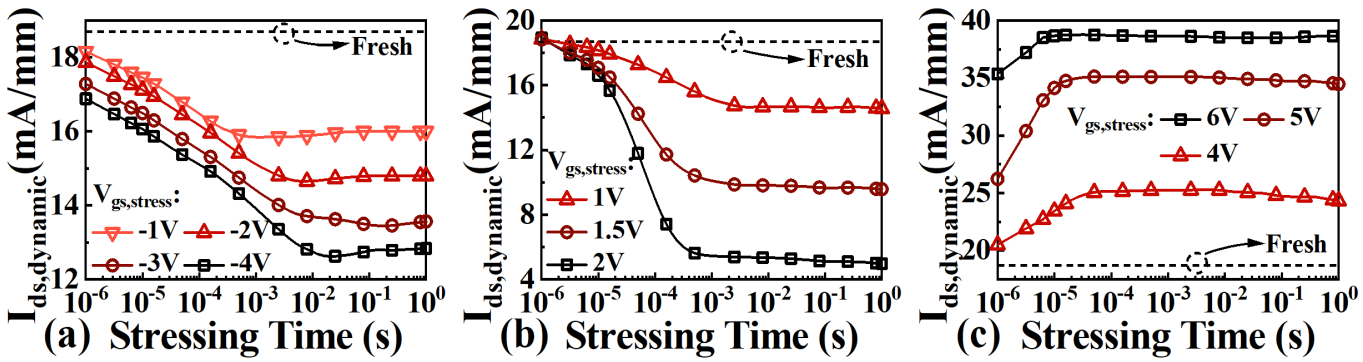

Fig. 3. (a)–(c) Drain current transient spectroscopy at 300 K for various negative/positive stressing voltages from −4 to 6 V. The drain current was measured at V_{gs} = 2 V and V_{ds} = 1 V.

III. Results and Discussion

Fig. 1(b) and (c) plotted transfer and transconductance characteristics of p-GaN gate AlGaN/GaN HEMT at room temperature. Threshold voltage (V_{th}) of this device was determined to be 1.45 V using 1 mA/mm standard (V_{ds} = 1 V, 300 K). Correspondingly, a maximum transconductance of 29.2 mS/mm was obtained at V_{ds} of 1 V. Fig. 1(d) illustrated output performance of this enhancement-mode GaN HEMT, which demonstrated a saturation current density of 218 mA/mm for V_{gs} = 5 V. In Fig. 1(e), as temperature was decreased to 140 K, the threshold voltage was barely shifted (1.45 V at 300 K and 1.51 V at 140 K). Fig. 1(f) shows ON-state gate current as a function of temperature, examined with V_{gs} = 5 V and V_{ds} = 1 V. The ON-state gate current was measured to be slightly higher than 10 mA/mm for a fully turned-on device. The gate current was reduced quickly when the temperature was below 240 K, although it was also observed that the threshold voltage was barely shifted as lowering the temperature. The reduction of the ON-state gate current was believed to be associated with reduction of hole tunneling current (when a highly doped p-GaN layer was used), which was resulted from decreased effective hole concentration in the p-GaN layer at low temperatures [25], [26]. Fig. 1(g) illustrated output performance of the p-GaN gate GaN HEMT from 300 to 140 K at V_{gs} = 5 V. The drain current increased for V_{ds} = 5 V as cooling down the device: 218 mA/mm at 300 K and 290 mA/mm at 140 K.

In Fig. 2, transfer curves under various gate bias stressing conditions were measured at 300 K with 1 V drain bias. Fig. 2(a) showed threshold voltage instability induced by negative gate bias, with stressing voltages from −2 to −4 V at room temperature. The threshold voltage was shifted positively as OFF-state stressing voltage was strengthened. With gate bias of −4 V for 1 s, a positive threshold voltage shift of 0.19 V was observed.

In Fig. 2(b), threshold voltage instability with low positive gate bias was investigated. Threshold voltage was found to be shifted fiercely: ΔV_{th} = 0.15 for 1 V stressing and ΔV_{th} = 0.57 for 2 V stressing. When p-GaN gate HEMT was stressed at high positive gate bias, threshold voltage was shifted negatively progressively, as shown in Fig. 2(c). For $V_{gs,stress}$ = 6 V, the threshold voltage was much lower than the original value (ΔV_{th} = −0.76 V). A complete mapping of the threshold voltage shift was summarized in Fig. 2(d).

Fig. 3 shows the time-resolved drain current at V_{gs} = 2 V and V_{ds} = 1 V as a function of gate bias stress and stressing duration. In Fig. 3(a), with a negative gate bias, dynamic drain current was decreased and finally reached a stable value as stressing time was extended. As the stressing gate bias was strengthened from −1 to −4 V, the ratio between dynamic

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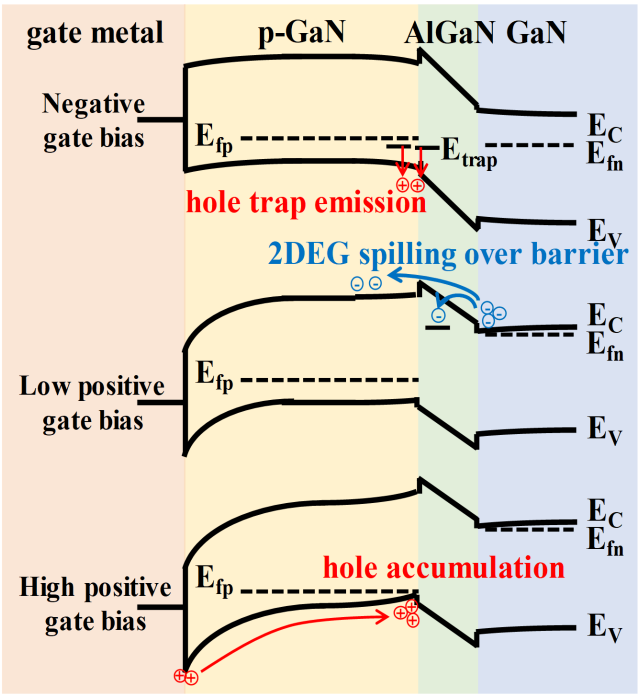

Fig. 4. Main mechanism causing p-GaN gate HEMT threshold voltage instability and drain current degradation/promotion under (i) negative gate bias, (ii) small positive gate bias, and (iii) large positive bias.

current and non-stressed value was reduced from 85% to 67%. And the time to reach a steady forward current was prolonged from 0.6 to 8.0 ms.

Fig. 3(b) revealed time-dependent results of dynamic drain current after positive gate voltage stressing of 1 to 2 V on p-GaN gate. The dynamic drain current after 2 V-gate stressing dropped to 27% of the fresh value due to severe threshold voltage shift. In Fig. 3(c), as the gate stressing voltage was further strengthened to 4 V or higher, the current was enhanced rather than being degraded due to negative shift of V_{th}.

The band diagram in Fig. 4 was used to pictorially explain the main mechanisms of the threshold voltage shift for a wide stressing range.

1) When negative gate bias was applied on the p-GaN gate, hole traps at the p-GaN/AlGaN interface, which were naturally filled, started to emit holes [3], [27]. De-trapped hole traps with negative charges would repel the carriers in the 2DEG channel, leading to positive shift of threshold voltage. As a result, decreased dynamic drain current was measured as the stressing process continued [Fig. 3(a)]. With a negative gate bias, negative gate leakage current was recorded in Table 1, in a good agreement with hole emission and extraction at the gate terminal.
2) When low positive gate bias ($V_{gs,stress}$ = 1–2 V) was applied, severe V_{th} shifts and drain current degradation were observed. This observation was related to the loss of carriers in the 2DEG channel due to upward moving of quasi-Fermi level with low positive gate bias. It is expected that electrons are able to escape from the channel as a result of AlGaN barrier lowering. Those electrons would recombine with holes in p-GaN layer or get trapped in AlGaN layer/p-GaN layer [17], [19]. The reduction of 2DEG caused a positive shift of threshold voltage and sharp current degradation at low gate bias.
3) While the gate was stressed at relatively high positive biases ($V_{gs,stress}$ > 4 V), the threshold voltage shifted negatively. The phenomenon was associated with increased hole injection from Schottky contact-based gate, leading to accumulation of holes at p-GaN/AlGaN interface [18], [28], [29]. The positive charge in gate-stack would result in an enhancement of 2DEG and negative shift of threshold voltage as well. As the gate bias was higher than 4 V, the gate leakage current kept increasing [Table 1], which indicated a strengthened hole injection process.

TABLE I
GATE LEAKAGE CURRENT DURING STRESSING PROCESS WITH VARIOUS $V_{GS,\ STRESS}$ AND ZERO DRAIN BIAS

$V_{gs,stress}$ (V)	-4	-3	-2	-1	1
I_g (mA/mm)	-0.031	-0.025	-0.021	-0.015	-0.005
$V_{gs,stress}$ (V)	2	3	4	5	6
I_g (mA/mm)	0.008	0.179	1.65	17.2	39.4

In short, for negative bias, the positive V_{th} shift corresponded to hole emission in p-GaN gate layer and partial depletion of the 2DEG. For small positive bias, positive shift of V_{th} and current degradation became much more severe due to spilled carriers from the channel. When high positive gate bias was applied to the device, V_{th} began to shift backward and dynamic drain current was enhanced, due to hole accumulation at the p-GaN/AlGaN interface and enlarged carrier density in the 2DEG channel.

Fig. 5(a)–(c) illustrated time-dependent recovery process at room temperature after stressing duration of 1 s. For these recovery processes after different gate bias stressing, drain current density returned to original values gradually, all within 30 ms. In the case of recovery after negative gate bias stressing [Fig. 5(a)], drain current typically remained unchanged until a recovery duration of 0.5 ms, for all the negative gate bias stressing conditions. After that, current recovery was gradually completed, which was associated with hole capturing process in p-GaN layer or AlGaN layer, a reverse process of the emission activities illustrated Fig. 4(a). In the case of recovery after low positive gate bias stressing in Fig. 5(b), the recovery process was linked to recovery of spilled 2DEG. In the case of recovery after large positive gate bias stressing, as shown in Fig. 5(c), the drain current recovered from enhanced current levels, corresponding to thermionic emission of accumulated holes at the interface of p-GaN/AlGaN.

Fig. 6(a) depicted temperature-dependent threshold voltage shift with fixed negative gate bias ($V_{gs,stress}$ = −4 V) for various stressing durations from 1 ms to 10 s. The threshold voltage was found to be continuously shifted positively as the stressing time was increased for each temperature step. The threshold voltage was stable after 100 ms stressing at 300 K.

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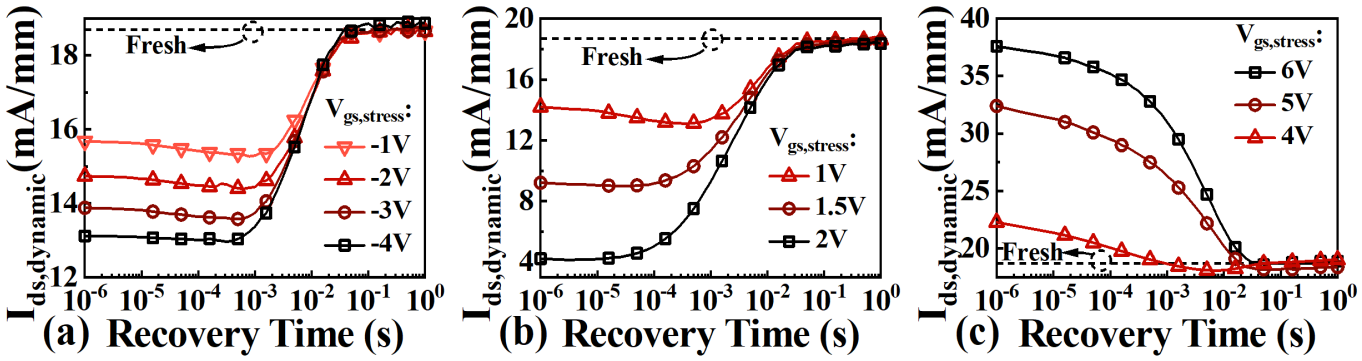

Fig. 5. (a)–(c) Drain current transient spectroscopy for the recovery process at 300 K after stressing at various negative/positive stressing voltages for 1 s. The drain current was measured at $V_{gs} = 2$ V and $V_{ds} = 1$ V.

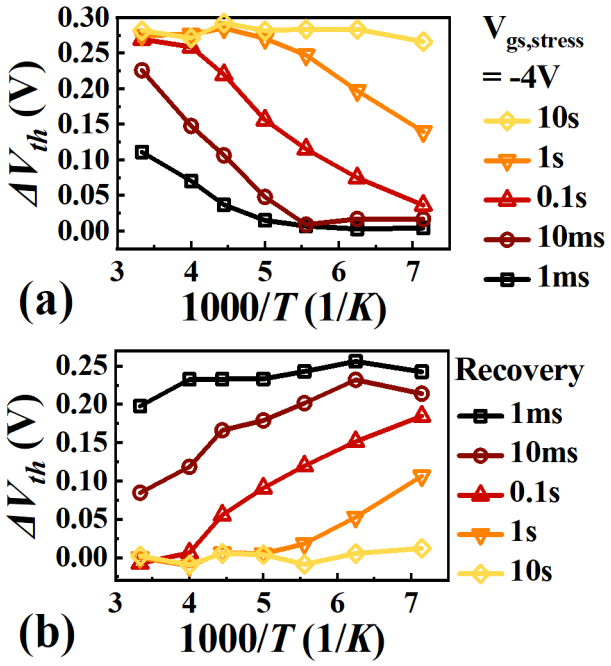

Fig. 6. (a) Negative bias induced threshold voltage instability (NBTI) under −4 V gate bias for different stress duration times (1 ms, 10 ms, 100 ms, 0.1 s, 1 s, and 10 s) from 300 to 140 K. (b) Threshold voltage recovery process with various duration periods ($V_{gs} = 0$ V, $V_{ds} = 0$ V) following gate bias stress ($V_{gs,\ stress} = -4$ V, 10 s).

At 140 K, it took 10 s for the device to reach a similar threshold voltage shift of 0.28 V. The results indicated that the time for stabilization of V_{th} with negative stressing was prolonged as decreasing the temperature. Meanwhile, Fig. 6(b) displayed the recovery process of threshold voltage after negative gate bias pre-stress ($V_{gs,stress} = -4$ V, 10 s). Typically, the time to achieve a certain amount of threshold voltage shift was also increased as the temperature was decreased. The process of recovery was finished within 10 ms at 300 K. As the temperature dropped to 140 K, the threshold voltage was nearly recovered after 10 s. During the recovery process, the hole traps in AlGaN started to capture holes and threshold voltage progressively returned to its original value. And the results suggested more active hole-capturing activities for hole traps in the p-GaN layer as heating up the device.

Fig. 7(a) showed extracted temperature-related and time-resolved drain current transient spectroscopy. Drain current was repeatedly probed at $V_{gs} = 5$ V and $V_{ds} = 1$ V during the stressing process with a fixed gate stressing voltage of −4 V. It is noted that although the dynamic current reduction was quite small (<2%) for a fully turned-on device ($V_{gs} = 5$ V), one may still extract activation energies for hole emission and capture process. As shown in Fig. 7(b), the transient process was illustrated using degradation ratio as defined as

$$\text{degradation ratio}(t) = \frac{I_{\text{dynamic, max}} - I_{\text{dynamic}}(t)}{I_{\text{dynamic, max}} - I_{\text{dynamic, min}}}. \quad (1)$$

The current degradation ratio showed that when the temperature decreases, the emission process associated with stressing was decelerated. The emission time constant was calculated to be 1.26 ms at 300 K and 100 ms at 180 K, based on the results of Fig. 7(a). The extended time constant revealed an inactive hole emission process as lowering the temperatures. Furthermore, an emission activation energy of 132 meV was extracted by the Arrhenius function [Fig. 7(b)], indicating an amount of energy was needed for acquiring hole carriers at the p-GaN/AlGaN interface. The recovery experiments were employed to reveal the temperature-dependent hole capture behaviors, as shown in Fig. 7(c). The recovery ratio in Fig. 7(c) was defined as

$$\text{recovery ratio}(t) = \frac{I_{\text{dynamic, max}} - I_{\text{dynamic}}(t)}{I_{\text{dynamic, max}} - I_{\text{dynamic, min}}}. \quad (2)$$

From 300 to 180 K, a slow-down drain current recovery process was identified. The capture time constant of holes was stretched from 6.3 ms at 300 K to 100 ms at 180 K. An activation energy of 70 meV was extracted for the recovery process, as shown in Fig. 7(d). The activation energy is comparable to the activation energy of 94 meV in Nardo *et al.*, [30], where dynamic R_{on} of p-GaN gate HEMT at OFF-state drain voltage stressing was monitored.

Fig. 8(a) depicted temperature-dependent threshold voltage instability after 6 V-gate-bias stressing for various durations (1 ms, 10 ms, 0.1 s, 1 s, and 10 s). With 1 ms-gate-stressing, the threshold voltage was shifted by around 0.8 V, but was

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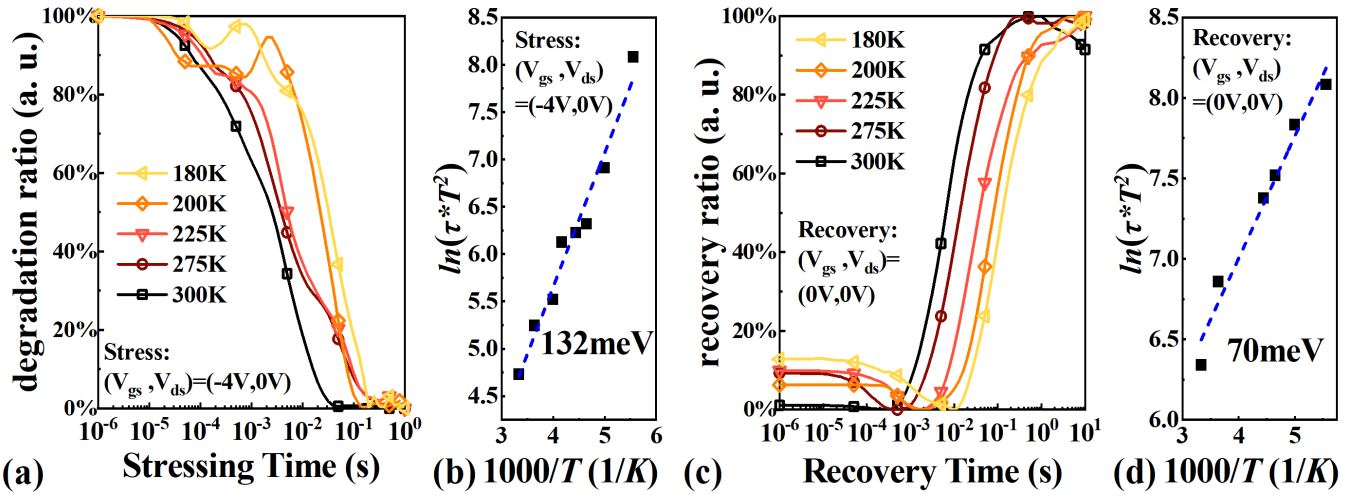

Fig. 7. (a) and (c) Extracted drain current transient spectroscopy under $V_{gs,\ stress} = -4$ V for various stressing/recovery times from 300 to 180 K. The drain current was measured at $V_{gs} = 5$ V and $V_{ds} = 1$ V. (b) and (d) Extracted activation energy from stressing/recovery process.

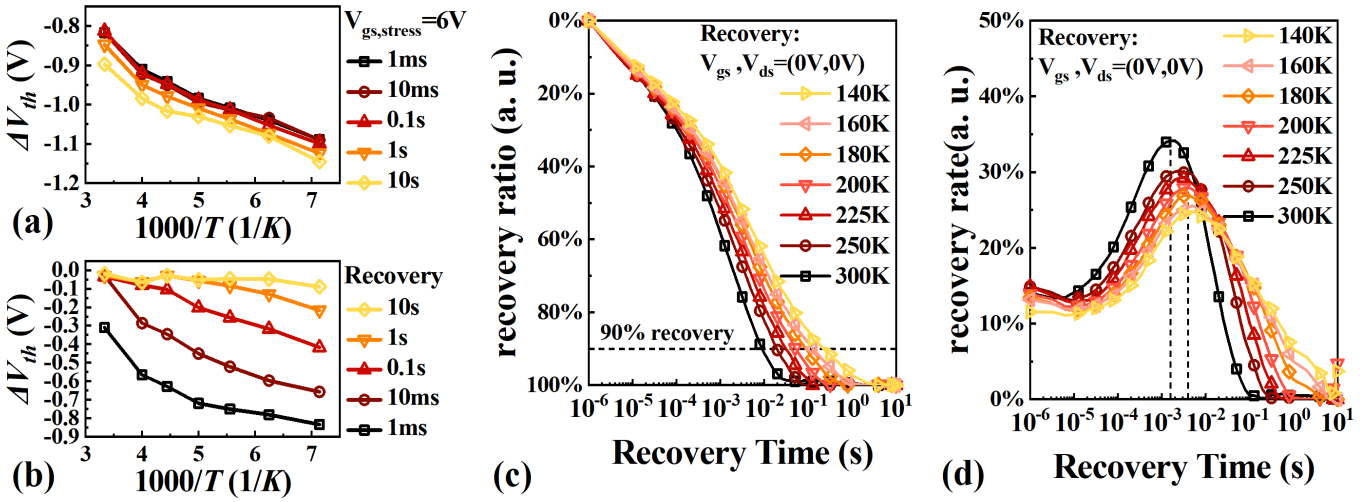

Fig. 8. (a) Positive bias-induced threshold voltage instability (PBTI) under 6 V gate bias for different stress duration times (1 ms, 10 ms, 100 ms, 0.1 s, 1 s, and 10 s) from 300 to 140 K. (b) Threshold voltage recovery process with various duration periods ($V_{gs} = 0$ V, $V_{ds} = 0$ V) following gate bias stress ($V_{gs,\ stress} = 6$ V, 10 s). (c) Extracted and absolutized recovery process under different duration periods after $V_{gs,\ stress} = 6$ V pre-stressing of 1 s from 300 to 140 K. The drain current was measured at $V_{gs} = 2$ V and $V_{ds} = 1$ V. (d) Extracted dynamic drain current recovery rate.

only slightly further shifted for a longer stressing duration. The results suggested a very fast hole accumulation process, in a good agreement with observations in Fig. 3(c). The devices showed more significant negative V_{th} shift at temperatures below 300 K. It was believed to be attributed to reduction of 2DEG spilling and/or enhancement of hole accumulation at high V_{gs} and at low temperatures. Fig. 8(b) revealed the extent of threshold voltage recovery, after applying a 10 s positive gate bias pre-stressing ($V_{gs,stress} = 6$ V). For each temperature step, threshold voltage was shifted toward its original value as recovery duration was extended, due to thermionic emission of accumulated holes at the p-GaN/AlGaN interface. It was also found that time of recovery was extended from 10 ms at 300 K to 10 s at 140 K, as a result of small thermal energy of the carriers at lower temperature.

Fig. 8(c) shows the temperature-dependent drain current transient spectroscopy after 1 s pre-stressing at 6 V ($V_{gs,\ stress} = 6$ V). At 300 K, it took 7 ms for drain current to have a 90% recovery. However, at 140 K it took 178 ms to complete the same process. This phenomenon was related to thermionic emission of accumulated holes at the interface of p-GaN and AlGaN.

Fig. 8(d) showed the recovery rate, which was obtained by taking the time derivate of the recovery ratio

$$\text{recovery rate}(t) = \frac{\partial(\text{recovery ratio}(t))}{\partial(\log_{10}(t))}. \tag{3}$$

From Fig. 8(d), one may extract corresponding recovery time constant for each temperature step, and note that the acquired time constant became slightly longer as lowering the

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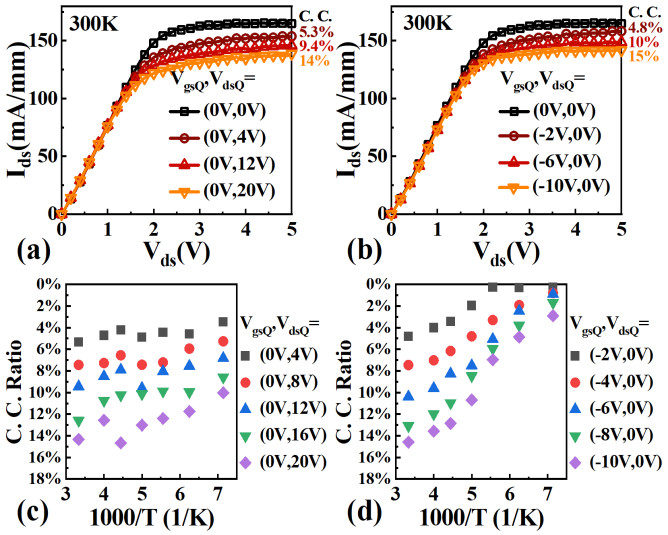

Fig. 9. (a) and (b) Pulsed output characteristics of p-GaN gate HEMTs with various drain–gate quiescent voltage at 300 K. The measurement V_{gs} was 5 V. (c) and (d) Extracted current collapse ratio of p-GaN gate HEMTs with various drain–gate quiescent voltage from 300 to 140 K.

temperature: 1.58 ms at 300 K and 3.96 ms for temperatures lower than 225 K.

Fig. 9(a) and (b) showed pulsed output characteristics with various quiescent voltages at 300 K. The gate bias during the ON-state was set as 5 V for fear of the influence of V_{th} shift. For (V_{gsQ}, V_{dsQ}) = (0, 4 V), the saturation current collapse ratio was measured to be 5.3%. As V_{dsQ} was increased to 20 V, the current collapse ratio was deteriorated to 14%. In Fig. 9(b), the drain quiescent voltage was fixed at 0 V and gate quiescent bias was set from 0 to −10 V. In the case of (V_{gsQ}, V_{dsQ}) = (−10, 0 V), the current collapse ratio was 15%: a similar degradation was observed when the potential difference between gate and drain was doubled as the case of (0, 20 V). The larger potential difference revealed that the gate stressing was more vital to the dynamic performance of the p-GaN gate HEMT at 300 K. As lowering the temperature, as shown in Fig. 9(c), the current collapse with certain drain quiescent bias was only slightly alleviated. For example, with stressing condition of (V_{gsQ}, V_{dsQ}) = (0, 20 V), the current collapse ratio was improved from 14.3% at 300 K to 10.0% at 140 K. However, as shown in Fig. 9(d), the current collapse with gate-only quiescent bias was much mitigated. In the case of (V_{gsQ}, V_{dsQ}) = (−10, 0 V), the current collapse ratio was reduced to 2.9% at 140 K, which is only 1/5 of the value at 300 K. The phenomenon is associated with slow-down hole de-trapping process at low temperature, which is consistent with observation in Fig. 7(a). It also suggests that the traps under the gate region rather than in the access region play a key role in determining the dynamic degradation.

Fig. 10(a) illustrated the pulsed output characteristics at V_{gs} = 2.5 V with various drain gate delay (DGD) and quiescent bias of (V_{gsQ}, V_{dsQ}) = (0, 8 V). DGD was defined as the time difference between a drain voltage reducing to V_{dsQ}/2 and V_{gsQ} reaching V_{th}. By precisely tuning the DGD, soft switch and hard switch could be well adjusted. For soft switching condition (DGD > 0), the current collapse

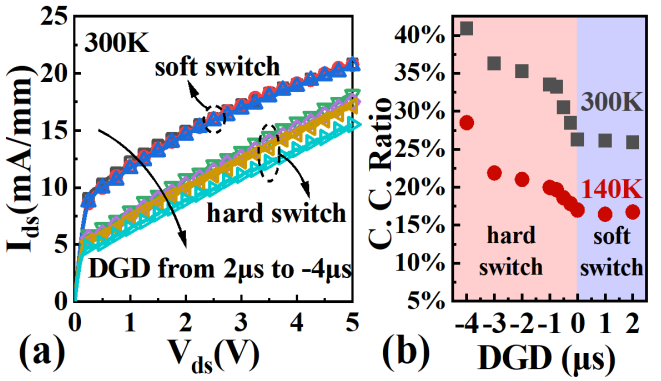

Fig. 10. (a) Pulsed output characteristics of p-GaN gate HEMTs with (V_{gsQ}, V_{dsQ}) = (0, 8 V) at 300 K for −4 to 2 μs DGD. The measurement V_{gs} was 2.5 V. (b) Current collapse ratio of hard switch and soft switch under 300 and 140 K.

was measured to be identically 26% regardless of the DGD value. For hard switching condition (DGD < 0), the current collapse was gradually deteriorated, as the DGD time was extended. The current collapse ratio was measured to be 41% for DGD of −4 μs. Extra current collapse observed in hard-switch mode of the p-GaN gate HEMT was believed to be caused by hot electron effect. High energy electrons which were accelerated by large drain bias would promote additional carrier capture in the AlGaN or in the buffer, leading to extra dynamic degradations [24]. Fig. 10(b) showed extracted current collapse ratio with various DGD at 300 and 140 K. For lower temperature, the current collapse under hard switch and soft switch was 27% and 16%, respectively. The hot electron effect could still be observed at low temperatures.

IV. Conclusion

DC and dynamic characteristics of p-GaN gate HEMT were thoroughly investigated for a wide temperature range. At 140 K, in addition to a negligibly shifted threshold voltage, a more-than doubled saturation drain current compared with the value at 300 K was observed. Gate bias induced threshold voltage instability could be divided into three stages depending on the gate bias polarity and strength. Hole trap emission, carrier out-spilling, and hole accumulation have been identified as major reasons for threshold voltage instability. Accordingly, the time-resolved drain current was also investigated. With 1 s pre-stressing for a wide gate bias from −4 to 6 V, it took less than 30 ms for the drain current to get full recovery. Temperature-dependent dynamic performance was investigated from 300 to 140 K. For negative gate bias, longer stressing time is needed to achieve certain level of V_{th} deviation from its original value as temperature was decreased. Via temperature-dependent drain current transient spectroscopy, time constant was extracted for both hole emission and hole capture process. Both time constants became larger as lowering the temperature. The hole emission activation energy and hole capture activation energy were extracted to be 132 and 70 meV, respectively. The emission time constant was prolonged from 1.26 ms (300 K) to 100 ms (140 K) as the temperature was decreased. For capture time

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constant, it was 6.3 ms at 300 K and 100 ms at 180 K, respectively. At 300 K, gate quiescent bias played a dominant role in current collapse compared with drain quiescent bias. Meanwhile, at low temperatures, massive alleviation of current collapse was observed in the case of mere gate quiescent bias. However, reduction of current collapse with drain quiescent bias at low temperature was less significant. When working in the hard-switch mode, the p-GaN HEMT showed additional current collapse than those in the soft-switching mode. It is believed energetic electrons which were accelerated by large drain-gate voltage promote additional carrier capture, leading to extra dynamic degradations.

ACKNOWLEDGMENT

Yitian Gu would like to acknowledge support from staff of Shanghaitech University Quantum Device Laboratory.

REFERENCES

[1] J. Wei *et al.*, "Charge storage mechanism of drain induced dynamic threshold voltage shift in p-GaN gate HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 526–529, Apr. 2019, doi: 10.1109/LED.2019.2900154.

[2] Y. Zhong *et al.*, "Normally-off HEMTs with regrown p-GaN gate and low-pressure chemical vapor deposition SiN_x passivation by using an AlN pre-layer," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1495–1498, Sep. 2019, doi: 10.1109/LED.2019.2928027.

[3] L. Efthymiou, K. Murukesan, G. Longobardi, F. Udrea, A. Shibib, and K. Terrill, "Understanding the threshold voltage instability during OFF-state stress in p-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1253–1256, Aug. 2019, doi: 10.1109/LED.2019.2925776.

[4] M. Meneghini *et al.*, "GaN-based power devices: Physics, reliability, and perspectives," *J. Appl. Phys.*, vol. 130, no. 18, Nov. 2021, Art. no. 181101, doi: 10.1063/5.0061354.

[5] W. B. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," *Electron. Lett.*, vol. 41, no. 7, pp. 449–450, Mar. 2005, doi: 10.1049/el:20050161.

[6] Y. Hao, L. Yang, X. Ma, J. Ma, M. Cao, C. Pan, C. Wang, and J. Zhang, "High-performance microwave gate-recessed AlGaN/AlN/GaN MOS-HEMT with 73% power-added efficiency," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 626–628, May 2011, doi: 10.1109/LED.2011.2118736.

[7] Y. Cai, Y. Zhou, K. M. Lau, and K. J. Chen, "Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based plasma treatment: From depletion mode to enhancement mode," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2207–2215, Sep. 2006, doi: 10.1109/TED.2006.881054.

[8] Z. Zhang *et al.*, "Normally off AlGaN/GaN MIS-high-electron mobility transistors fabricated by using low pressure chemical vapor deposition Si_3N_4 gate dielectric and standard fluorine ion implantation," *IEEE Electron Device Letters*, vol. 36, no. 11, pp. 1128–1131, Nov. 2015, doi: 10.1109/LED.2015.2483760.

[9] I. Hwang *et al.*, "p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 202–204, Feb. 2013, doi: 10.1109/LED.2012.2230312.

[10] H. Jiang, R. Zhu, Q. Lyu, and K. M. Lau, "High-voltage p-GaN HEMTs with off-state blocking capability after gate breakdown," *IEEE Electron Device Lett.*, vol. 40, pp. 530–533, Feb. 2019, doi: 10.1109/LED.2019.2897694.

[11] C.-H. Chang, Y.-C. Lin, J.-S. Niu, W.-S. Lour, J.-H. Tsai, and W.-C. Liu, "High-performance AlGaN/GaN enhancement-mode high electron mobility transistor by two-step gate recess and electroless-plating approaches," *Sci. Adv. Mater.*, vol. 13, no. 1, pp. 30–35, Jan. 2021, doi: 10.1166/sam.2021.3823.

[12] F. Albany *et al.*, "Stability of the threshold voltage in fluorine-implanted normally-off AlN/GaN HEMTs co-integrated with commercial normally-on GaN HEMT technology," *Microelectron. Rel.*, vol. 126, Nov. 2021, Art. no. 114291, doi: 10.1016/j.microrel.2021.114291.

[13] Y. Huang *et al.*, "High-performance normally off p-GaN gate high-electron-mobility transistor with $In_{0.17}Al_{0.83}N$ barrier layer design," *Opt. Quantum Electron.*, vol. 53, no. 3, p. 139, Mar. 2021, doi: 10.1007/s11082-021-02786-2.

[14] H.-C. Chiu *et al.*, "High-performance normally off p-GaN gate HEMT with composite $AlN/Al_{0.17}Ga_{0.83}N/Al_{0.3}Ga_{0.7}N$ barrier layers design," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 201–206, 2018, doi: 10.1109/JEDS.2018.2789908.

[15] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, "Mechanism of threshold voltage shift in p-GaN gate AlGaN/GaN transistors," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1145–1148, Aug. 2018, doi: 10.1109/LED.2018.2847669.

[16] J. He, J. Wei, S. Yang, M. Hua, K. Zhong, and K. J. Chen, "Temperature-dependent gate degradation of p-GaN gate HEMTs under static and dynamic positive gate stress," in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, 2019, pp. 295–298, doi: 10.1109/ISPSD.2019.8757574.

[17] Y. Shi *et al.*, "Carrier transport mechanisms underlying the bidirectional V_{TH} shift in p-GaN gate HEMTs under forward gate stress," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 876–882, Feb. 2019, doi: 10.1109/TED.2018.2883573.

[18] A. Stockman, E. Canato, M. Meneghini, G. Meneghesso, P. Moens, and B. Bakeroot, "Threshold voltage instability mechanisms in p-GaN gate AlGaN/GaN HEMTs," in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 287–290, doi: 10.1109/ISPSD.2019.8757667.

[19] J. He, G. Tang, and K. J. Chen, "V_{TH} instability of p-GaN gate HEMTs under static and dynamic gate stress," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1576–1579, Oct. 2018, doi: 10.1109/LED.2018.2867938.

[20] X. Li *et al.*, "Observation of dynamic V_{TH} of p-GaN gate HEMTs by fast sweeping characterization," *IEEE Electron Device Lett.*, vol. 41, no. 4, pp. 577–580, Apr. 2020, doi: 10.1109/LED.2020.2972971.

[21] C. Zhang, S. Li, S. Liu, J. Wei, W. Wu, and W. Sun, "Electrical degradations of p-GaN HEMT under high off-state bias stress with negative gate voltage," in *Proc. IEEE 26th Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA)*, Jul. 2019, pp. 1–4, doi: 10.1109/IPFA47161.2019.8984885.

[22] L. Nela, N. Perera, C. Erine, and E. Matioli, "Performance of GaN power devices for cryogenic applications down to 4.2 k," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, Jul. 2021, doi: 10.1109/TPEL.2020.3047466.

[23] F. Masin *et al.*, "Charge trapping and stability of E-mode p-gate GaN HEMTs under soft- and hard-switching conditions," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2020, pp. 1–4, doi: 10.1109/IRPS45951.2020.9129116.

[24] Y. Gu, Y. Wang, J. Chen, B. Chen, M. Wang, and X. Zou, "Temperature-dependent dynamic degradation of carbon-doped GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3290–3295, Jul. 2021, doi: 10.1109/TED.2021.3077345.

[25] L. Efthymiou, G. Longobardi, G. Camuso, T. Chien, M. Chen, and F. Udrea, "On the physical operation and optimization of the p-GaN gate in normally-off GaN HEMT devices," *Appl. Phys. Lett.*, vol. 110, no. 12, Mar. 2017, Art. no. 123502, doi: 10.1063/1.4978690.

[26] I. C. Kizilyalli and O. Aktas, "Characterization of vertical GaN p–n diodes and junction field-effect transistors on bulk GaN down to cryogenic temperatures," *Semicond. Sci. Technol.*, vol. 30, no. 12, Dec. 2015, Art. no. 124001, doi: 10.1088/0268-1242/30/12/124001.

[27] J. Chen *et al.*, "OFF-state drain-voltage-stress-induced V_{TH} instability in Schottky-type p-GaN gate HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3686–3694, Jun. 2021, doi: 10.1109/JESTPE.2020.3010408.

[28] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold voltage instability in p-GaN gate AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2454–2460, Jun. 2018, doi: 10.1109/TED.2018.2828702.

[29] E. Canato *et al.*, "μs-range evaluation of threshold voltage instabilities of GaN-on-Si HEMTs with p-GaN gate," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2019, pp. 1–6, doi: 10.1109/IRPS.2019.8720549.

[30] A. Nardo *et al.*, "Non thermally-activated transients and buffer traps in GaN transistors with p-type gate: A new method for extracting the activation energy," *Microelectron. Rel.*, vol. 114, Nov. 2020, Art. no. 113842, doi: 10.1016/j.microrel.2020.113842.

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