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Voltage-Controlled Reconfigurable Boolean Logic Enabled by a β-Ga_2O_3 Artificial Optoelectronic Synapse

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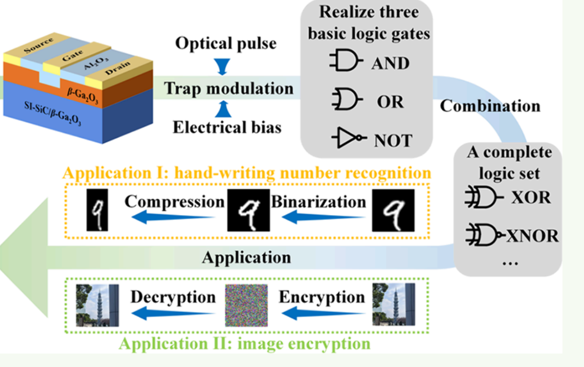
ABSTRACT: Reconfigurable Boolean logics have garnered significant attention due to their potential to meet growing requirements of low energy consumption, short time delay, and high integrated circuit density in digital systems. Synaptic devices present a promising candidate toward reconfigurable Boolean logic gates by adjusting terminal biases, particularly working with optical stimulus. In this work, an optoelectronic synaptic device based on a β-Ga_2O_3 metal-oxide−semiconductor field effect transistor (MOSFET) for reconfigurable Boolean logic gates is demonstrated via a trap-carrier modulation scheme. Synaptic functionalities including excitatory postsynaptic current (EPSC), paired-pulse facilitation (PPF), and transition from short-term memory (STM) to long-term memory (LTM) are investigated. For a single EPSC, the β-Ga_2O_3 optoelectronic synaptic device exhibits low energy consumption (E_{con}) and excellent noise immunity. In addition, AND, OR, and NOT gates are implemented by tuning terminal voltages. Combing the reconfigurable logic functions and synaptic behaviors of the β-Ga_2O_3 MOSFET, two typical applications, namely, handwriting number recognition and image encryption, are explicitly investigated. The validation of trap-modulated β-Ga_2O_3 synaptic devices for reconfigurable Boolean logic gates paves a solid path for high-performance digital systems.



KEYWORDS: *β-Ga_2O_3, optoelectronic artificial synapse, reconfigurable Boolean logic, handwriting number recognition, image encryption*

INTRODUCTION

In recent years, digital integrated circuits serve as an indispensable element in electronics industry such as mobile phones, electric vehicles, and so on.[1,2] Nevertheless, at present the aforementioned fields exert a rising expectation of lower energy consumption, shorter time delays, and higher integrated circuit density for digital systems.[3] One promising solution toward increasing integrated circuit density together with low energy consumption is utilizing reconfigurable Boolean logic gates,[4,5] which enables incorporation of multiple logic functions within a single device.[6,7] AND/NAND, OR/NOR, and NOT gates are considered to be three basic logic gates, which could compose complicated logic functions by combining basic logic operations. Reconfigurable Boolean logic functions of AND, OR, and NOT gates have been successfully demonstrated with ultralow energy consumption via a dual-gated MoS_2 transistor.[5]

In previous studies, reconfigurable Boolean logic gates were realized via distinct reconfiguration methods.[5,8−10] Initialization is a common method to initialize reconfigurable Boolean logic gates.[5,11,12] Fourteen Boolean logic functions were implemented via initialization and writing with merely aJ-level energy consumption,[11] whereas initialization inevitably led to extra reconfiguration time between the Boolean logic functions. Zhu et al. achieved temperature-induced spiking AND to OR gate transformation by indium−gallium−zinc-oxide (IGZO) based transistors,[8] in conjunction with the challenge to accurately alter the temperature of each single device within integrated chips. Sun et al. demonstrated the implementation of XOR and XNOR gates, regarding current and resistance as the output of two Boolean logic gates, respectively,[9] which unavoidably demanded two receiver systems and increased circuit complexity. In contrast, voltage-controlled reconfigurable Boolean logic represents a promising approach for a simple reconfiguration process and avoidance of initialization.[4,13] NOT and NOR gates have been successfully realized in a voltage-controlled field effect transistor (FET),[4] while the absence of the AND/NAND gate impedes the attainment of complicated logic functions.

Besides the application for artificial vision systems and sound perception,[14,15] synaptic devices also hold immense potential

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for reconfigurable Boolean logic gates.[16] Excitatory post-synaptic current (EPSC) can be flexibly modulated with the variation of optical intensity, optical pulse number, and optical pulse width (t_{Po}).[6,17−19] Trap-modulated synaptic devices exhibit the advantage of high repeatability and low leakage current,[20] together with the high plasticity of EPSC by voltage-modulated trap behavior.[21] Deep level traps are also widely observed in β-Ga_2O_3,[22−24] offering huge adjustable probability and diversity of synaptic behavior. AND, NAND, OR, and NOR gates have been successfully realized by a two-terminal fully photon-modulated synaptic device based on a β-Ga_2O_3/ZnO heterojunction.[16] Nevertheless, the reconfiguration between distinct logic functions necessitates prior setup of light illumination, resulting in extra reconfiguration time. Meanwhile, voltage-controlled reconfigurable Boolean logics have also been demonstrated by two-terminal synaptic devices, in spite of being limited to the functions of AND and OR gates,[6] with the NOT gate missing. A complete logic function set with a simple reconfiguration method is missing based on prior Ga_2O_3-based optoelectronic synapses. By comparison, three-terminal synaptic devices provide the possibility for a complete logic function set due to the enhanced flexibility to modulate the synaptic behaviors and logic outputs by gate input and drain input, particularly working with an optical stimulus.[21]

In this paper, an optically stimulated β-Ga_2O_3 synaptic device on a SiC substrate for reconfigurable Boolean logic gates is fabricated. With the optical pulse, synaptic behaviors such as EPSC, paired-pulse facilitation (PPF), and long-term memory (LTM) are observed in the β-Ga_2O_3 metal-oxide−semiconductor field effect transistor (MOSFET). It is also revealed that EPSC can be modulated flexibly by drain voltage (V_{DS}) and gate voltage (V_{GS}), and three basic Boolean logic gates including AND, OR, and NOT gates are attained on a single β-Ga_2O_3 MOSFET, contributing to the composition of complicated Boolean logic functions. With the reconfigurable Boolean logic function and other synaptic behavior, two typical applications, namely, handwriting number recognition and image encryption, are investigated. The results reveal the huge application potential Boolean for reconfigurable logic based on a β-Ga_2O_3 artificial optoelectronic synapse.

■ EXPERIMENTAL SECTION

Figure 1a displays the schematic of the biological synapse and synaptic device. The devices were fabricated on a β-Ga_2O_3/SiC heterogeneous integrated wafer, which was fabricated from a 2 in. β-Ga_2O_3 wafer and a 4 in. 4H-SiC wafer. Hydrogen ions were implanted into the β-Ga_2O_3 wafer to form a damage layer, and the two wafers were bonded together by hydrophilic wafer bonding. A β-Ga_2O_3 thin film was exfoliated from the 4H-SiC substrate after annealing at 450 °C with atmospheric pressure. More detailed information on the fabrication process of the β-Ga_2O_3/SiC heterogeneous integrated wafer was published in previous works.[25,26] The manufactory process contained five major steps: mesa isolation, ion implantation, recess channel, ohmic contact formation, and gate stack formation. Inductively coupled plasma-reactive ion etching (ICP-RIE) was utilized to form the mesa isolation. The β-Ga_2O_3 conductive channel was implanted by Si ions and recessed to achieve an enhancement mode β-Ga_2O_3 MOSFET. Ti/Au (20/160 nm) was deposited by electron-beam evaporation (EBE), followed by rapid thermal annealing (RTA) at 475 °C for 60 s to form an ohmic contact. A 30 nm-thick Al_2O_3 was deposited by atomic layer deposition (ALD), and a Ni/Au (20/160 nm) Schottky contact was formed by EBE. More detailed information on the fabrication process of the β-Ga_2O_3 MOSFET was reported in previous works.[25]

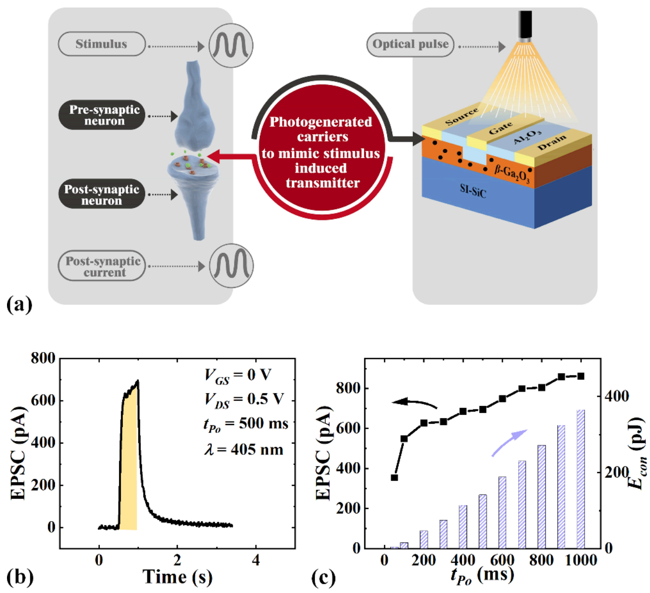

Figure 1. a) Schematic of biological synapse and synaptic device. b) EPSC stimulated by optical pulse. c) EPSC and energy consumption (E_{con}) with various t_{Po}.

■ RESULTS AND DISCUSSION

The image of the β-Ga_2O_3 MOSFET from an optical microscope is exhibited in Supporting Information (Figure S1). The device features a gate length (L_G) of 2 μm, a gate−source distance (L_{GS}) of 4 μm, a gate−drain distance (L_{GD}) of 16 μm, and a gate width (W_G) of 20 μm. The electrical characteristics of the β-Ga_2O_3 MOSFET are shown in Supporting Information (Figure S2). A threshold voltage (V_{th}) of 10.69 V is extracted by the linear extrapolation method at a V_{DS} of 5 V.

In a biological system, synapses serve as the conduits for information transmission between the presynaptic neuron and the postsynaptic neuron.[27] With the stimulus of a biological signal, information transmission begins with the exocytosis of neurotransmitters triggered in the presynaptic neurons to the synaptic clefts. Through synaptic clefts, neurotransmitters are received by the receptors on postsynaptic neurons, thereby inducing excitatory postsynaptic currents (EPSCs).[21] To mimic a biological system by the β-Ga_2O_3 MOSFET, a gate electrode and β-Ga_2O_3 conductive channel connected with a drain electrode and source electrode are considered as the presynaptic neuron and postsynaptic neuron, respectively, and optical pulses induced by a laser with a wavelength (λ) of 405 nm are regarded as biological stimuli. As shown in Figure 1b, the EPSC is evoked by a presynaptic optical pulse spiking with a t_{Po} value of 500 ms. V_{GS} and V_{DS} are held at 0 and 0.5 V, respectively. With optical excitation, a peak current amplitude of 696 pA is observed. Subsequent to the optical pulse, optical-induced current gradually decreases, resembling a decay like a biological EPSC. Upon the application of an optical pulse to the β-Ga_2O_3 MOSFET held in the off state, photogenerated electron−hole pairs are excited in the β-Ga_2O_3 conductive channel. Trap states capture a number of photogenerated carriers, and the remaining photogenerated carriers are accumulated in the β-Ga_2O_3 conductive channel. Positive V_{DS} forms the electric field from drain to source, leading to the amplification of photoexcited current, denoted as EPSC. Upon cessation of the optical pulse, the current decreases owing to the swift recombination process of carriers, while trapped carriers require more time to be released, resulting in the gradual decrease. More detailed EPSC with various t_{Po}, EPSC repeatability, and cycle-to-cycle stability results are shown in the Supporting Information (Figure S3). EPSC values with errors below 5% reveal the excellent EPSC repeatability and cycle-to-cycle stability of the β-Ga_2O_3 MOSFET. As exhibited in Figure 1c, EPSC and E are described as a function of t_{Po}. The increase of EPSC from 354 to 862 pA indicates an augmented number of accumulated photogenerated carriers during longer t_{Po} from 50 to 1000 ms. For each EPSC, E_{con} can be calculated by the following eq 1:[28]

$$\int \mathrm{d}E_{con} = \int V_{DS} \times I_{DS} \times \mathrm{d}t \tag{1}$$

where t represents the time during the optical pulse. As shown in Figure 1c, the β-Ga_2O_3 synaptic device exhibits a notable benefit in terms of low E_{con}, which remains below 400 pJ even with t_{Po} extended to 1000 ms and reaches 4.56 pJ with a t_{Po} of 50 ms. Meanwhile, the on/off ratio and signal-to-noise ratio (SNR) also reveal the anti-interference performance of synaptic devices, which are shown in the Supporting Information (Figure S4). The on/off ratio of EPSC is defined as the ratio of current under an optical pulse (I_{ph}) and dark current (I_{dark}) and reaches 94.41 with a t_{Po} of 1000 ms. The SNR can be expressed by the following eq 2:[29]

$$\mathrm{SNR} \geq 10\,\mathrm{lg}\left(\frac{I_{EPSC}}{\sigma_{noise}}\right) \tag{2}$$

where I_{EPSC} and σ_{noise} are the peak amplitude of the current and the standard deviation of the noise, respectively. The SNR reaches 23.40 dB at a t_{Po} of 1000 ms. High on/off ratio and SNR demonstrate the excellent noise immunity of the β-Ga_2O_3 MOSFET.

In neuroscience, temporal enhancement in synaptic connection is considered short-term plasticity (STP). Regarded as a typical STP, PPF characterizes the capability of a biological synapse to process the temporal signals.[30,31] In biological systems, the second EPSC exhibits a larger amplitude than the first one when employing two continuous stimuli. Analogous to the synaptic device, two adjacent optical pulses are considered as two biological stimuli. As shown in Figure 2a, employing two adjacent optical pulses with a t_{Po} of 50 ms and t_{int} of 300 ms, the PPF index, which is defined as the ratio of the second EPSC (A_2) response to the first EPSC (A_1),[32] reaches 1.57, demonstrating the heightened second EPSC subsequent to two adjacent optical pulses, resembling short-term plasticity (STP) in neuroscience. The results can be explained by trap behaviors. When the first optical pulse is applied on the device, photogenerated carriers are accumulated in the β-Ga_2O_3 conductive channel or captured by trap states. Upon cessation of the first optical pulse, the emission process of trapped carriers leads to a gradual decrease compared to the sharp increase during the optical pulse. With the second optical pulse applied before the fulfillment of the emission process, fewer empty trap states occur in the device and fewer photogenerated carriers are captured by traps, contributing to an augmented accumulation of carriers occurring in the β-Ga_2O_3 conductive channel and an enhanced EPSC during the second optical pulse.

As plotted in Figure 2b, the reduction of PPF index from 1.78 to 1.33 indicates that more carriers are released during

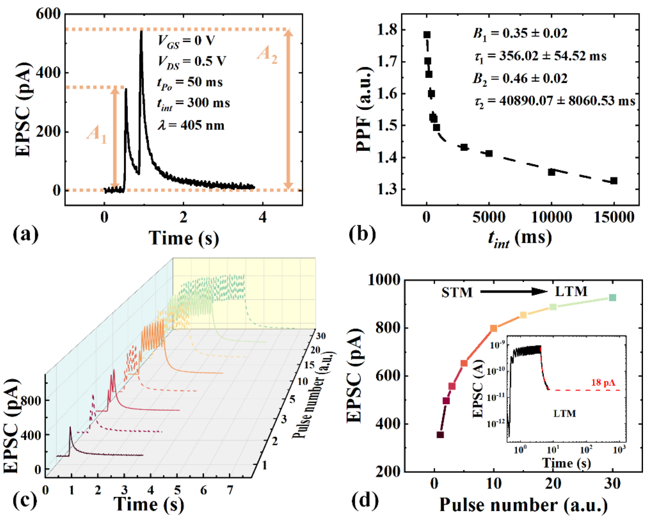

Figure 2. a) EPSC with two adjacent optical pulses. b) PPF as a function of interval time (t_{int}). c) EPSC stimulated by multiple optical pulses. d) EPSC with pulse number from 1 to 30. Inset: fitting of the EPSC with 30 optical pulses.

prolonged t_{int} from 50 to 15000 ms, and the number of remaining carriers for the second EPSC decreases. According to previous studies, the PPF index can be described by the following eq 3:[33−37]

$$\mathrm{PPF} = B_1 e^{-t_{int}/\tau_1} + B_2 e^{-t_{int}/\tau_2} + 1 \tag{3}$$

where B_1 and B_2 represent the ratio of the current magnitudes in fast and slow stages, respectively, and τ_1 and τ_2 represent the characteristic relaxation times of fast and slow phases, respectively. As shown in Figure 2b, the fitting matches well with the experimental results. B_1 and B_2 are calculated to be 0.34 ± 0.02 and 0.46 ± 0.02, respectively, and τ_1 and τ_2 are calculated to be 356.02 ± 54.52 and 40980.07 ± 8060.53 ms, respectively. In biological synapses, τ_2 is 2 orders of magnitude larger than τ_1, matching well with our results.[38] The fitting of PPF demonstrates the excellent STP of our synaptic devices as biological short-term memory (STM).

Figure 2c illustrates EPSC with pulse numbers from 1 to 30. EPSC increases as pulse number rises, attributed to the increasing accumulation in the β-Ga_2O_3 conductive channel. Meanwhile, with continuous rehearsal, the memory effect is consolidated repeatedly, and STM will be converted to LTM,[39,40] which is caused by the capture process of deep trap states. As plotted in Figure 2d, when the pulse number is less than 3, the EPSC remains below 600 pA, representing that only a few carriers are accumulated in the β-Ga_2O_3 conductive channel alongside occupancy of shallow trap states during optical pulses. After optical pulses, the filled shallow trap states take a small amount of time to release the carriers, representing STM of the β-Ga_2O_3 MOSFET. With further stimulation, EPSC reaches 927 pA after 30 optical pulses and needs more time to release, suggesting that the memory effect is strengthened by continuous optical pulses. When the pulse number further increases, carriers begin to be captured by deep level trap states, and the extended release time required for carriers trapped by deep trap states forms LTM of the β-Ga_2O_3 MOSFET. The reduction process of the EPSC can be fitted to validate the LTM effect.[41] As displayed in the inset of Figure 2d, the results reveal that EPSC is maintained at about 18 pA

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for a long time, while the dark current level is lower than 3 pA, underscoring the excellent LTM of the β-Ga_2O_3 MOSFET.

Besides t_{Po}, the EPSC can also be modulated by tuning terminal voltages. Figure 3a displays EPSC with a V_{DS} spanning from 0.25 to 1.25 V in increments of 0.25 V. The peak EPSC value at V_{DS} of 1.25 V is much higher than it is at V_{DS} of 0.25 V, indicating that although a larger drain−source electric field strength improves the capture process of trap states in the access region, the generation of electron−hole pairs is highly enhanced as well, leading to the enhanced accumulation. As shown in Figure 3b, with a V_{GS} of 0 V and t_{Po} of 50 ms, a substantial enhancement of 236.15% is signified when V_{DS} increases from 0.25 to 1.25 V, demonstrating a huge adjustment scope. The enhancement is also investigated with a t_{Po} from 100 to 1000 ms, which is shown in the Supporting Information (Figure S5). Figure 3c plots EPSC with a V_{GS} spanning from −1 V to 1 V in increments of 0.5 V. As shown in Figure 3d, when V_{GS} assumes positive values, EPSC increases with rising V_{GS}. The enhancement of the EPSC implies that a larger gate−source electric field strength also augments the generation of electron−hole pairs and the accumulation of carriers. However, an EPSC of around 10 pA is significantly suppressed with a negative V_{GS} of −0.5 V and −1 V. The distinct phenomenon observed with various V_{GS} can be elucidated by trap behaviors. When a positive V_{GS} is employed, trap states are filled due to the positive electric field from gate to source and narrow depletion region. Only a limited number of trap states possess the capacity to capture photogenerated carriers, leading to a notable accumulation in the β-Ga_2O_3 conductive channel. Conversely, the negative V_{GS} prompts the emission process of trap states due to the negative electric field from source to gate and the broad depletion region. During the optical pulse, the large amount of empty trap states captures the photogenerated carriers, suppressing

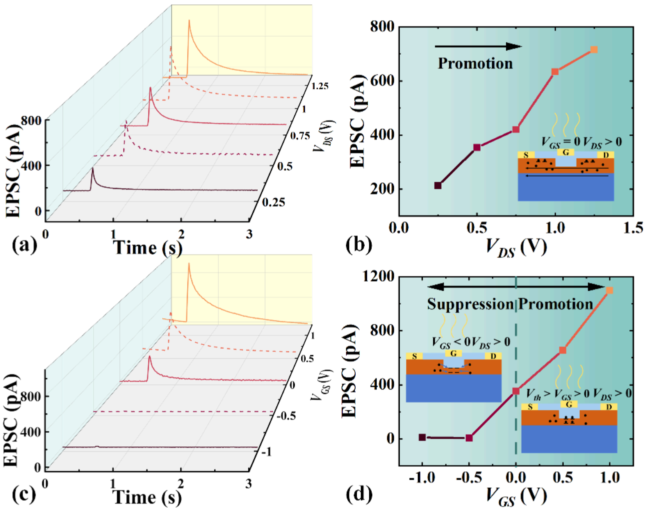
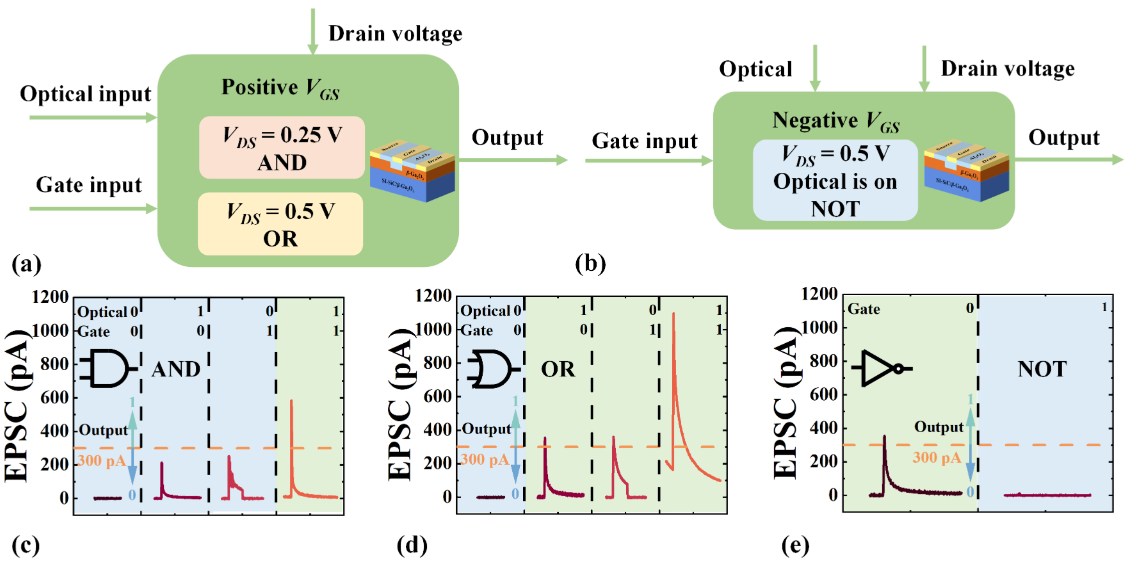


Figure 3. a) EPSC at a V_{GS} of 0 V. b) Peak EPSC value modulated by a V_{DS} from 0.25 to 1.25 V. Inset: the schematic of trap behaviors when $V_{DS} > 0$. c) EPSC at a V_{DS} of 0.5 V. d) Peak EPSC value modulated by a V_{GS} from −1 to 1 V. Inset: the schematic of trap behaviors when $V_{th} > V_{GS} > 0$ and $V_{GS} < 0$.



	AND				OR				NOT	
Optical input	0	0	1	1	0	0	1	1	-	-
Gate input	0	1	0	1	0	1	0	1	0	1
Output	0	0	0	1	0	1	1	1	1	0

(f)

Figure 4. Schematic of a) AND, OR, and b) NOT gates. The corresponding EPSC of the c) AND gate, d) OR gate, and e) NOT gate, in which the blue background and green background mean outputs of 0 and 1, respectively. f) The truth table of three logic gates.

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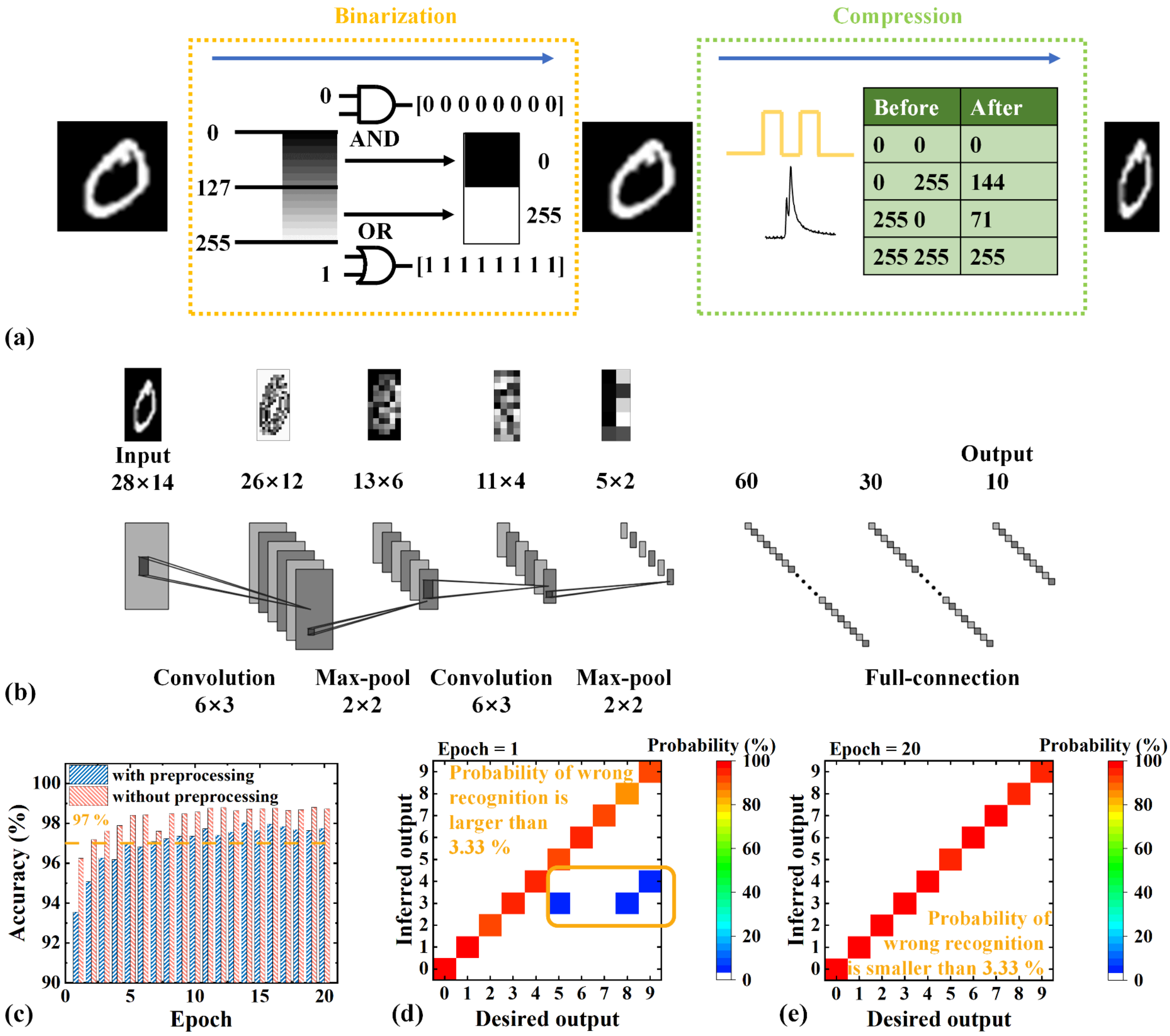
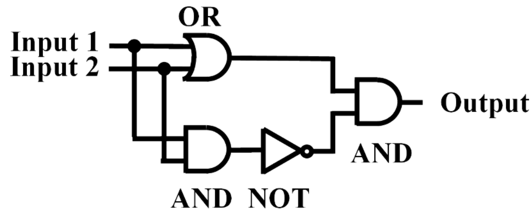


Figure 5. a) Preprocessing stage which contains the binarization process and compression process. b) The structure of a convolutional neural network (CNN) for handwriting number recognition after preprocessing. c) The accuracy of the CNN model with epochs from 1 to 20 before and after preprocessing. The confusion matrix of recognition for images after preprocessing with epochs of d) 1 and e) 20.

the number of residual carriers in the β-Ga_2O_3 conductive channel, and the negative electric field from gate to source will suppress the generation of electron−hole pairs as well, resulting in imperceptible EPSC with a negative V_{GS}.

On the basis of the capacity to modulate EPSC by tuning terminal voltages, the implementation of reconfigurable Boolean logic gates becomes feasible. In this study, the β-Ga_2O_3 MOSFET mimics three basic logic gates—AND, OR, and NOT gates—by modulating trap behaviors via optical and electrical inputs. Figure 4a and b displays the schematic of three basic logic gates. When V_{DS} is maintained at 0.25 V and a positive V_{GS} of 1 V and optical pulse with a t_{P_o} of 50 ms are considered as two inputs, β-Ga_2O_3 MOSFET operates as an AND gate with a threshold current of 300 pA. With the same condition except for a V_{DS} of 0.5 V, the operating function of the β-Ga_2O_3 MOSFET transforms to an OR gate. Meanwhile, the NOT gate function can be mimicked with a negative V_{GS} of −1 V as the input, a V_{DS} of 0.5 V, and an optical pulse. The measurement results are plotted in Figure 4c, d, and e, in which the blue background and green background signify the scenarios of outputs of 0 and 1, respectively, and Figure 4f shows the truth table of three basic logic gates. The realization of AND, OR, and NOT gates demonstrates enormous potential in digital integrated chips.

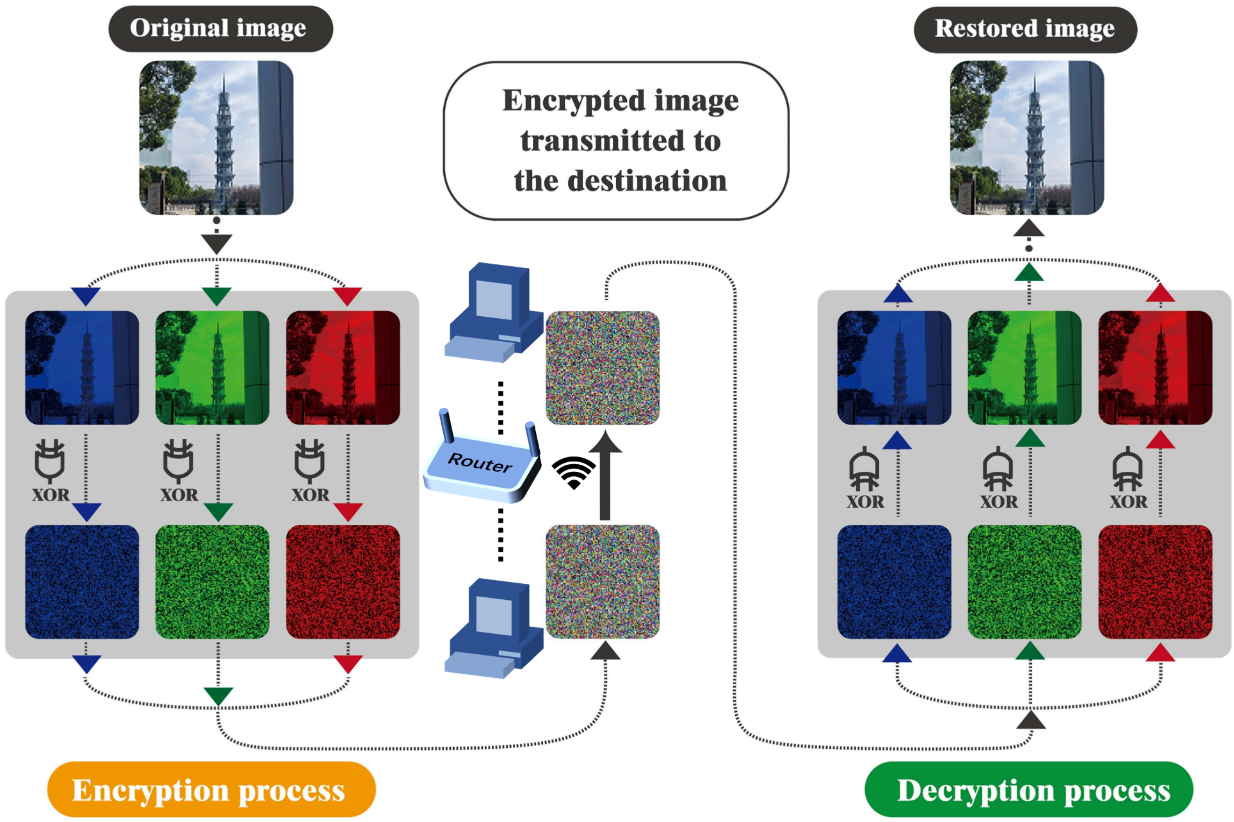
Artificial vision systems, one of the most important applications of neuromorphic computing, have attracted huge attention in previous studies.[42,43] The reconfigurable Boolean logic functional β-Ga_2O_3 synaptic devices can be used for preprocessing information. In this study, a Modified National Institute of Standards and Technology (MNIST) data set and a CNN model are employed to assess the efficacy of the β-Ga_2O_3 MOSFET. Figure 5a displays the preprocessing stage, which consists of the binarization process and compression process. In the binarization process, 28 × 28 MNIST handwritten digital images are binarized to be images containing only 0 and 255 gray-level with a threshold of 127 gray-level, in which each gray-level will be converted to an 8-bit binary number. If the gray-level is smaller than 127, the 8-bit binary number of the gray-level and binary number 0 are considered as two inputs of the AND gate, and the output will be an 8-bit binary number [0 0 0 0 0 0 0 0], representing a 0 gray-level. Conversely, if the gray-level is larger than 128, the OR gate and binary number 1 will be used to achieve an 8-bit binary number [1 1 1 1 1 1 1 1], representing a 255 gray-level. Meanwhile, the β-Ga_2O_3 MOSFET can also be utilized in the



(a)

	XOR			
Input 1	0	0	1	1
Input 2	0	1	0	1
Output	0	1	1	0

(b)



(c)

Figure 6. a) Circuit of the XOR gate. b) The truth table of the XOR gate. c) The encryption process of the color image by logic gates based on the synaptic device.

compression process via PPF behavior. During the compression process, 28 × 28 binarized images are compressed to be 28 × 14 images, in which two adjacent pixels in a row can be regarded as an optical pulse train. For instance, [255 255] means two adjacent optical pulses, and [0 0] means no optical pulse. After that, two adjacent pixels in a row can be encoded to a new gray-level by the specific current value of the β-Ga_2O_3 MOSFET. As exhibited in Figure 5b, a CNN model with two convolution layers, two max-pool layers, and three full-connection layers is used to validate the recognition accuracy. A total of 60000 images and an extra 10000 images after preprocessing are utilized as the training images and testing images, respectively. The variation of number zero at each stage is exhibited in Figure 5a and b, and more detailed information about the other nine numbers is shown in Supporting Information (Figure S6). For comparison, the same images without the preprocessing stage and the corresponding CNN model are considered as the reference experiment. The accuracy after preprocessing as a function of epoch is plotted in Figure 5c, together with a reference result of images without a preprocessing stage. The CNN model exhibits excellent performance for images with and without a preprocessing stage and achieves the accuracy of 93.55% and 96.24% with an epoch of 1, respectively. With further training, the accuracy for images with and without a preprocessing stage stabilizes above 97% and 98% and reaches 97.74% and 98.73% with an epoch of 20, respectively. The recognition accuracy without preprocessing is a little larger than that with preprocessing, and the reasonable and tolerable difference stabilizes at 1% due to less information for the CNN model after the compression process. Nevertheless, the compression process also causes lower computational load, which leads to lower demand for computational power. Figure 5d displays the confusion matrix for recognition of 10000 test images after preprocessing with an epoch of 1, and only a few blue grids exist, which represents that the probability of wrong recognition is larger than 3.33%. As shown in Figure 5e, when the epoch reaches 20, no blue grid is observed, indicating that the probability of each wrong recognition after preprocessing is smaller than 3.33%, representing an exceptional performance. A more detailed

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performance is displayed in Supporting Information (Figure S7). The results infer huge potential for the deployment of the β-Ga_2O_3 MOSFET in visual recognition.

Studies on devices for the preprocessing stage in artificial vision systems are summarized in Supporting Information (Table S1). Compared to the common function of a sensor in the sensing stage, most previous reports in artificial vision systems focus on the training stage and the preprocessing stage.[18,39,44−47] Among them, an outstanding preprocessing stage brings the advantages of increasing recognition accuracy and saving training time. Our preprocessing stage saves computational power and training time with almost no decrease of accuracy.

Complex logic units can be made up of three fundamental logic gates, such as NOR, NAND, XOR, and XNOR gates, which can be used in many scenarios such as image encryption.[48] Although they are unavailable with a single β-Ga_2O_3 MOSFET due to the limitation of modulation parameters, based on three fundamental logic gates, NOR, NAND, XOR, and other complex logic units can also be realized by the combination of several β-Ga_2O_3 MOSFETs. In this study, image encryption is validated based on the XOR gate, which consists of two AND gates, one OR gate, and one NOT gate, as shown in Figure 6a. Compared to the XOR gate based on a complementary metal−oxide−semiconductor (CMOS),[49,50] reconfigurable Boolean logic gates based on an artificial optoelectronic synapse exhibit less complexity and higher flexibility. Figure 6b displays the truth table of the XOR gate. The prepared 100 × 100 color image for encryption can be decomposed into three monochromatic images of three primary colors: red, green, and blue. Each monochromatic image contains 10000 pixels from 0 to 255, equivalent to 10000 8-bit binary numbers. For each 8-bit binary number, an 8-bit secret key is generated randomly and stored for the decryption process. Each bit of the 8-bit binary number and the corresponding bit of the 8-bit secret key are regarded as two inputs of the XOR gate, respectively, and the XOR gate exports an 8-bit encrypted binary number. In all, 30000 8-bit secret keys are created to encrypt three monochromatic images, which are finally composed into the encrypted color image. As exhibited in Figure 6c, the encrypted color image completely eliminates the feature of the original color image, demonstrating the outstanding encryption ability of the β-Ga_2O_3 MOSFET. The decryption process is the same as the encryption process, which completely restores the original color image successfully.

Table 1 summarizes some synaptic devices for logic functions. Compared to some studies based on two-terminal devices, which only realize one or two basic logic functions,[6,51] our three-terminal synaptic device realizes three basic logic gates, AND, OR, and NOT, leading to a complete logic function set. Based on our synaptic devices, more complex logic functions could be integrated, leading to some complicated applications. Some studies also realize more than three logic functions,[5,16] while the preprocessing stage such as high initial current and the set/reset process is necessary for the reconfiguration between different logic functions, and extra reconfiguration time inevitably exists between the logic functions. In contrast, our reconfiguration method avoids extra time and holds an advantage of simple operation, due to the avoidance of initialization and temperature variation.[5,8,16] A complete logic function set is formed based on the β-Ga_2O_3 MOSFET with a simple reconfiguration method of voltage modulation.

Table 1. Comparison of Synaptic Devices for Logic Functions

Material	Terminal number	Boolean logic	Reconfiguration method
β-Ga_2O_3 (This work)	Three	AND, OR, NOT	Voltage
Ga_2O_3[6]	Two	AND, OR	Voltage
β-Ga_2O_3[51]	Two	IMP	-
β-Ga_2O_3/ZnO[16]	Two	AND, OR, NOR, NAND	Initialization
MoS_2[5]	Four	AND, OR, NOT	Initialization
IGZO[8]	Three	AND, OR	Temperature

The β-Ga_2O_3-based synaptic devices and memristor are summarized in Supporting Information (Table S2). Compared to the memristors based on 2D material and organic materials, optoelectronic synaptic devices based on β-Ga_2O_3 MOSFETs exhibit high flexibility to modulate synaptic behavior.

■ CONCLUSIONS

In this work, a β-Ga_2O_3 optoelectronic synaptic device for reconfigurable Boolean logic gates is demonstrated. Via a 405 nm light pulse as stimulation, the β-Ga_2O_3 MOSFET exhibits typical synaptic behaviors such as EPSC, PPF, and transition from STM to LTM. In a single EPSC, a low E_{con} of only 8.85 pJ at a t_{Po} of 50 ms is calculated, and on/off ratio and SNR reach 94.41 and 23.40 dB at a t_{Po} of 1000 ms, respectively, demonstrating the excellent noise immunity. Three basic Boolean logic gates, AND, OR, and NOT, are also successfully implemented by a single β-Ga_2O_3 MOSFET, resulting in the integration of complicated logic functions. Based on the Boolean logic function and other synaptic behaviors of the β-Ga_2O_3 MOSFET, two typical applications are illustrated. The capability of image binarization by AND and OR gates and image compression by PPF before visual recognition is demonstrated by a CNN model. Meanwhile, the application of image encryption is also validated by the XOR gate. The typical applications reveal immense potential of the utilization of trap-modulated β-Ga_2O_3 synaptic devices for reconfigurable Boolean logic gates in high-performance digital systems.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.5c01613.

Image of β-Ga_2O_3 MOSFET from an optical microscope (Figure S1), output curves and transfer curves of β-Ga_2O_3 MOSFET (Figure S2), EPSC as a function of t_{Po}, EPSC repeatability and cycle-to-cycle stability (Figure S3), on/off ratio and SNR of EPSC (Figure S4), EPSC as a function of t_{Po} with V_{DS} from 0.25 to 0.75 V and corresponding contour map (Figure S5), detailed example of variation process of 10 numbers during preprocessing stage and CNN model (Figure S6), the confusion matrix for recognition with various epochs (Figure S7), comparison of devices for preprocessing stage in artificial vision systems (Table S1), and comparison of β-Ga_2O_3-based synaptic devices and memristors (Table S2) (PDF)

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Notes

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REFERENCES

(1) Markov, I. L. Limits on fundamental limits to computation. *Nature* **2014**, *512* (7513), 147−154.

(2) Tang, G.; Kwan, A. M. H.; Wong, R. K. Y.; Lei, J.; Su, R. Y.; Yao, F. W.; Lin, Y. M.; Yu, J. L.; Tsai, T.; Tuan, H. C.; Kalnitsky, A.; Chen, K. J. Digital Integrated Circuits on an E-Mode GaN Power HEMT Platform. *IEEE Electron Device Lett.* **2017**, *38* (9), 1282−1285.

(3) Kim, J.; Jung, M.; Lim, D. U.; Rhee, D.; Jung, S. H.; Cho, H. K.; Kim, H.-K.; Cho, J. H.; Kang, J. Area-Selective Chemical Doping on Solution-Processed MoS_2 Thin-Film for Multi-Valued Logic Gates. *Nano Lett.* **2022**, *22* (2), 570−577.

(4) Sahoo, S.; Varghese, A.; Sadashiva, A.; Goyal, M.; Sakhuja, J.; Bhowmik, D.; Lodha, S. Vertically Integrated Dual-Memtransistor Enabled Reconfigurable Heterosynaptic Sensorimotor Networks and In-Memory Neuromorphic Computing. *ACS Nano* **2025**, *19* (13), 13287−13299.

(5) Du, J.-y.; Ge, C.; Riahi, H.; Guo, E.-j.; He, M.; Wang, C.; Yang, G.-z.; Jin, K.-j. Dual-Gated MoS_2 Transistors for Synaptic and Programmable Logic Functions. *Adv. Electron. Mater.* **2020**, *6* (5), 1901408.

(6) Cui, D.; Pei, M.; Lin, Z.; Zhang, H.; Kang, M.; Wang, Y.; Gao, X.; Su, J.; Miao, J.; Li, Y.; Zhang, J.; Hao, Y.; Chang, J. Versatile optoelectronic memristor based on wide-bandgap Ga_2O_3 for artificial synapses and neuromorphic computing. *Light Sci. Appl.* **2025**, *14* (1), 161.

(7) Song, X.; Li, C.; Zhong, X.; Zhang, R.; Ji, T.; Liu, X.; Wu, W.; Zhang, H.; Liu, L.; Chen, N.; Zhang, J.; Dai, Z.; Ye, Y.; Ren, X.; Yao, J. Gate and Bias Voltage-Modulation Photodetector Based on $Cs_3Bi_2Br_9$ for Multifunctional Optoelectronic Logic Gate. *Adv. Funct. Mater.* **2025**, *35*, 2502415.

(8) Zhu, Y.; He, Y.; Chen, C.; Zhu, L.; Wan, C.; Wan, Q. IGZO-based neuromorphic transistors with temperature-dependent synaptic plasticity and spiking logics. *Sci. China Inf. Sci.* **2022**, *65* (6), 162401.

(9) Sun, Y.; Li, Z.; Li, Q.; Yuan, Q.; Wang, Y.; Li, B. Synaptic devices based on organic ferroelectric memtransistor with arithmetic calculating and logic functions. *Electrochim. Acta* **2024**, *473*, 143512.

(10) Guo, P.; Zhang, J.; Hua, Z.; Sun, T.; Li, L.; Dai, S.; Xiong, L.; Huang, J. Organic Synaptic Transistors Based on a Semiconductor Heterojunction for Artificial Visual and Neuromorphic Functions. *Nano Lett.* **2025**, *25* (8), 3204−3211.

(11) Zhao, R.; Liu, H.; Yang, M.; Lu, T.; Li, Z.; Shi, Z.; Wang, Z.; Liu, J.; Yang, Y.; Ren, T.-L. Reconfigurable aJ-Level Ferroelectric Transistor-Based Boolean Logic for Logic-in-Memory. *Nano Lett.* **2024**, *24* (35), 10957−10963.

(12) Quhe, R.; Di, Z.; Zhang, J.; Sun, Y.; Zhang, L.; Guo, Y.; Wang, S.; Zhou, P. Asymmetric conducting route and potential redistribution determine the polarization-dependent conductivity in layered ferroelectrics. *Nat. Nanotechnol.* **2024**, *19* (2), 173−180.

(13) Yuan, S.; Feng, Z.; Qiu, B.; Li, Y.; Zhai, P.; Li, L.; Wu, Z.; Ma, S.; Xu, B.; Ding, L.; Wei, G.; Shen, G. Silicon carbide nanowire-based multifunctional and efficient visual synaptic devices for wireless transmission and neural network computing. *Sci. China Mater.* **2023**, *66* (8), 3238−3250.

(14) Yang, C.; Sun, B.; Zhou, G.; Guo, T.; Ke, C.; Chen, Y.; Shao, J.; Zhao, Y.; Wang, H. Photoelectric Memristor-Based Machine Vision for Artificial Intelligence Applications. *ACS Mater. Lett.* **2023**, *5* (2), 504−526.

(15) Wei, Y.; Liu, Y.; Lin, Q.; Liu, T.; Wang, S.; Chen, H.; Li, C.; Gu, X.; Zhang, X.; Huang, H. Organic Optoelectronic Synapses for Sound Perception. *Nano-Micro Lett.* **2023**, *15* (1), 133.

(16) Sun, S.; Zhang, T.; Jin, S.; Pan, X.; Lu, J.; Ye, Z.; Lu, B. Fully UV Modulated Artificial Synapses with Integrated Sensing, Storage and Computation. *Adv. Funct. Mater.* **2024**, *34* (36), 2401403.

(17) Li, J.; Feng, Z.; Qian, Y.; Huang, W.; Li, W.; Ling, H.; Yi, M.; Zhao, Q. Organic Semiconductor Heterojunction-Based Photonic Synaptic Transistor with Temperature Stability and Adaptive Learning Ability for Neuromorphic Computing Systems. *ACS Appl. Electron. Mater.* **2025**, *7* (13), 6149−6157.

(18) Cao, X.; Wu, Y.; Li, W.; Gu, J.; Xu, S.; Deng, W.; Chen, Z.; Yang, L. Transparent Optoelectronic Synapse Device Based on the Bi_2O_3/ZnO Heterojunction for Neuromorphic Computing. *ACS Appl. Electron. Mater.* **2025**, *7* (14), 6332−6341.

https://doi.org/10.1021/acsaelm.5c01613
ACS Appl. Electron. Mater. XXXX, XXX, XXX−XXX

(19) Yao, J.; Teng, Y.; Wang, Q.; He, Y.; Liu, L.; Zhao, C.; Kang, L. Advancing Intelligent Neuromorphic Computing: Recent Progress in All-Optical-Controlled Artificial Synaptic Devices. *ACS Nano* **2025**, *19* (29), 26320−26346.

(20) Lee, G.; Baek, J.-H.; Ren, F.; Pearton, S. J.; Lee, G.-H.; Kim, J. Artificial Neuron and Synapse Devices Based on 2D Materials. *Small* **2021**, *17* (20), 2100640.

(21) Chen, J.; Du, H.; Qu, H.; Gao, H.; Gu, Y.; Zhu, Y.; Ye, W.; Zou, J.; Wang, H.; Zou, X. AlGaN/GaN MOS-HEMT enabled optoelectronic artificial synaptic devices for neuromorphic computing. *APL Mach. Learn.* **2024**, *2* (2), No. 026113.

(22) Polyakov, A. Y.; Nikolaev, V. I.; Yakimov, E. B.; Ren, F.; Pearton, S. J.; Kim, J. Deep level defect states in β-, α-, and ε-Ga_2O_3 crystals and films: Impact on device performance. *J. Vac. Sci. Technol. A* **2022**, *40* (2), No. 020804.

(23) Wang, Z.; Chen, X.; Ren, F.-F.; Gu, S.; Ye, J. Deep-level defects in gallium oxide. *J. Phys. D: Appl. Phys.* **2021**, *54* (4), No. 043002.

(24) Qu, H.; Chen, J.; Zhang, Y.; Sui, J.; Gu, Y.; Deng, Y.; Su, D.; Zhang, R.; Lu, X.; Zou, X. Emission and capture characteristics of electron trap (E_{emi} = 0.8 eV) in Si-doped β-Ga_2O_3 epilayer. *Semicond. Sci. Technol.* **2023**, *38* (1), No. 015001.

(25) Qu, Z.; Xie, Y.; Zhao, T.; Xu, W.; He, Y.; Xu, Y.; Sun, H.; You, T.; Han, G.; Hao, Y.; Ou, X. Extremely Low Thermal Resistance of β-Ga_2O_3 MOSFETs by Co-integrated Design of Substrate Engineering and Device Packaging. *ACS Appl. Mater. Interfaces* **2024**, *16* (42), 57816−57823.

(26) Shen, Z.; Xu, W.; Chen, Y.; Lin, J.; Xie, Y.; Huang, K.; You, T.; Han, G.; Ou, X. Wafer-scale single-crystalline β-Ga_2O_3 thin film on SiC substrate by ion-cutting technique with hydrophilic wafer bonding at elevated temperatures. *Sci. China Mater.* **2023**, *66* (2), 756−763.

(27) Jo, E. S.; Rim, Y. S. Assessment of trapping layer control in IGZO/Al_2O_3/Ga_2O_3 synaptic transistor for neuromorphic computing. *Mater. Today Phys.* **2023**, *37*, 101194.

(28) Chen, X.; Mi, W.; Li, M.; Tang, J.; Zhao, J.; Zhou, L.; Zhang, X.; Luan, C. Optoelectronic artificial synapses based on β-Ga_2O_3 films by RF magnetron sputtering. *Vacuum* **2021**, *192*, 110422.

(29) Guo, L. Q.; Han, H.; Zhu, L. Q.; Guo, Y. B.; Yu, F.; Ren, Z. Y.; Xiao, H.; Ge, Z. Y.; Ding, J. N. Oxide Neuromorphic Transistors Gated by Polyvinyl Alcohol Solid Electrolytes with Ultralow Power Consumption. *ACS Appl. Mater. Interfaces* **2019**, *11* (31), 28352−28358.

(30) Long, Z.; Ding, Y.; Poddar, S.; Gu, L.; Zhang, Q.; Fan, Z. Bio-inspired visual systems based on curved image sensors and synaptic devices. *Mater. Today Electron.* **2023**, *6*, 100071.

(31) Liu, X.; Huang, W.; Kai, C.; Yin, L.; Wang, Y.; Liu, X.; Pi, X.; Yang, D. Photogated Synaptic Transistors Based on the Heterostructure of 4H-SiC and Organic Semiconductors for Neuromorphic Ultraviolet Vision. *ACS Appl. Electron. Mater.* **2023**, *5* (1), 367−374.

(32) Zhang, G.; Liu, W.; Huo, N.; Zheng, Z.; Zhang, M.; Liu, X.; Luo, D.; Yang, M.; Gao, W. Vertical Monolithic SiC Optoelectronic Synapses with Visible-Light Neuromorphic Plasticity. *ACS Appl. Electron. Mater.* **2025**, *7* (14), 6560−6569.

(33) Yoon, Y.; Kim, Y.; Hwang, W. S.; Shin, M. Biological UV Photoreceptors-Inspired Sn-Doped Polycrystalline β-Ga_2O_3 Optoelectronic Synaptic Phototransistor for Neuromorphic Computing. *Adv. Electron. Mater.* **2023**, *9* (7), 2300098.

(34) Gao, F.; Wang, T.; Bai, J.; Gong, W.; Jiang, Y.; Zhang, X.; Li, L. Amorphous Ga_2O_3 Based Erasable Two-Terminal Artificial Photonic Synapses. *Adv. Opt. Mater.* **2025**, *13* (12), 2403227.

(35) Wang, Z.; Zhang, G.; Zhang, X.; Wu, C.; Xia, Z.; Hu, H.; Wu, F.; Guo, D.; Wang, S. Polarization-Sensitive Artificial Optoelectronic Synapse Based on Anisotropic β-Ga_2O_3 Single Crystal for Neuromorphic Vision Systems and Information Encryption. *Adv. Opt. Mater.* **2024**, *12* (29), 2401256.

(36) Zhang, Y.; Huang, Y.; Huang, C.; Yang, Y.; Li, Z.; Wang, Y.; Luo, L.; Wu, C. Plasma-Engineered AlGaN/GaN Optoelectronic Synapses for Low-Power Neuromorphic Computing. *Adv. Opt. Mater.* **2025**, *13* (13), 2403370.

(37) Jeong, H.; Ahn, D.-H.; Park, S.; Ju, G.; Han, J.-H.; Kim, Y. Visible Light Wavelength-Dependent Erasing in AOS-Based Charge Trap TFTs for Enhanced Neuromorphic Display Performance. *ACS Appl. Electron. Mater.* **2025**, *7* (12), 5463−5472.

(38) Fan, W.; Yan, H.; Wang, X.; Tong, L.; Yan, W.; Su, C.; Wang, Q.; Yin, S. Polarization-Sensitive Photosynapse Based on $PdSe_2$/WS_2 Heterostructure for Visible-Infrared Broadband Artificial Vision System. *Adv. Funct. Mater.* **2025**, 2416703.

(39) Shrivastava, S.; Keong, L. B.; Pratik, S.; Lin, A. S.; Tseng, T.-Y. Fully Photon Controlled Synaptic Memristor for Neuro-Inspired Computing. *Adv. Electron. Mater.* **2023**, *9* (3), 2201093.

(40) Zhang, Y.; Wang, L.; Yang, M.; Lin, D.; Wang, B.; Zhang, N.; Jiang, Z.; Liu, M.; Zhu, Z.; Hu, H. Multiposition Controllable Gate WS_2/MoS_2 Heterojunction Phototransistor and Its Applications in Optoelectronic Logic Operation and Emulation of Neurotransmission. *Adv. Opt. Mater.* **2022**, *10* (12), 2200197.

(41) Kai, C.; Wang, Y.; Liu, X.; Liu, X.; Zhang, X.; Pi, X.; Yang, D. AlGaN/GaN-Based Optoelectronic Synaptic Devices for Neuromorphic Computing. *Adv. Opt. Mater.* **2023**, *11* (7), 2202105.

(42) Youn, S.; Hwang, Y.; Kim, T.-H.; Kim, S.; Hwang, H.; Park, J.; Kim, H. Threshold learning algorithm for memristive neural network with binary switching behavior. *Neural Netw.* **2024**, *176*, 106355.

(43) Cao, D.-w.; Yan, Y.; Wang, M.-n.; Luo, G.-l.; Zhao, J.-r.; Zhi, J.-k.; Xia, C.-x.; Liu, Y.-f. Layered Wide Bandgap Semiconductor $GaPS_4$ as a Charge-Trapping Medium for Use in High-Temperature Artificial Synaptic Applications. *Adv. Funct. Mater.* **2024**, *34* (28), 2314649.

(44) Yin, Z.; Shan, L.; Ci, R.; Hao, D.; Miao, G.; Tian, L.; Liu, G.; Shan, F. Visible light-driven synaptic transistors based on bilayer InGaZnO homojunction for neuromorphic computing. *Appl. Phys. Lett.* **2025**, *126* (10), 103302.

(45) Zhou, G.; Li, J.; Song, Q.; Wang, L.; Ren, Z.; Sun, B.; Hu, X.; Wang, W.; Xu, G.; Chen, X.; Cheng, L.; Zhou, F.; Duan, S. Full hardware implementation of neuromorphic visual system based on multimodal optoelectronic resistive memory arrays for versatile image processing. *Nat. Commun.* **2023**, *14* (1), 8489.

(46) Deng, W.; Yu, Y.; Yan, X.; Wang, L.; Yu, N.; Liao, X.; Luo, W.; Wu, J. Linearly Programmable Oxygen-Doped MoS_2 Memtransistor for Neuromorphic Computing. *ACS Nano* **2025**, *19* (30), 27526−27537.

(47) Zhao, S.; Hou, X.; Cheng, Y.; Zhang, Q.; Zhao, J.; Tao, L. Optical Synaptic Devices with Multiple Encryption Features Based on SERS-Revealed Charge-Transfer Mechanism. *Adv. Mater.* **2025**, *37* (24), 2503146.

(48) Guo, B.; Chen, X.; Chen, A.; Wang, J.; Xue, W.; Wang, T.; Wu, Z.; Zhong, X.; Zeng, J.; Li, J.; Li, M.; Xu, X.; Chen, Y.; Liu, G. Molecular HDD logic for encrypted massive data storage. *Nat. Commun.* **2025**, *16* (1), 2046.

(49) Sharma, U.; Jhamb, M. A Novel Design of Voltage and Temperature Resilient 9-T Domino Logic XOR /XNOR Cell. *Circuits Syst. Signal Process.* **2022**, *41* (11), 6314−6332.

(50) Liu, L.; Hu, W.; Yang, Z.; Wei, Y.; Peng, C.; Wu, X.; Lin, Z.; Lu, W.; Zhou, Y.; Chen, J. A high charge-discharge stability SRAM 10T1C XOR CIM macro applied in BCAM and Hamming distance. *Microelectron. J.* **2025**, *161*, 106718.

(51) Li, R.; Lin, Y.; Li, Y.; Gao, S.; Yue, W.; Kan, H.; Zhang, C.; Shen, G. Amorphous gallium oxide homojunction-based optoelectronic synapse for multi-functional signal processing. *J. Semicond.* **2023**, *44* (7), No. 074101.

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ACS Appl. Electron. Mater. XXXX, XXX, XXX−XXX